I. INTRODUCTION

This paper discusses the background, applications, and proposed characterization of Gallium Nitride (GaN) based hybrid MOS-HEMTs for high-voltage power switching. The basic material properties, device structure, and basics of operation are discussed in section II. Section III touches on the relevance and motivation behind this research and some simple examples of where GaN based MOS-HEMTs would be used. Section IV outlines an experimental plan to characterize newly designed and fabricated MOS-HEMTs in order to compare their performance and design tradeoffs with previously fabricated devices and current state of the art MOS-HEMTs.

II. BACKGROUND

Gallium Nitride (GaN) has been touted to be a great semiconductor for high-voltage, high frequency, and high-temperature devices thanks to its excellent material properties including its wide bandgap (3.4eV), large critical electric field (3MV/cm), and good thermal conductivity (1.3 W/cm-K) when compared with Silicon (Si) and Silicon Carbide (SiC) [1]. Additionally a two-dimensional electron gas (2DEG) can be formed via an AlGaN/GaN heterostructure solely from spontaneous and piezoelectric induced polarization charge (requires no doping like in AlGaAs/GaAs HEMTs) [2]. It should be noted that bulk GaN is very difficult and expensive to grow, thus the majority of GaN devices are fabricated on epitaxially grown GaN on Sapphire, Silicon Carbide, or Silicon substrates.

For high-voltage switching applications the tradeoff between specific on resistance (Ron,sp) and breakdown voltage is a critical design tradeoff that must be addressed. Additionally power switching devices should be normally off for safety and reliability purposes. AlGaN/GaN HEMTs provide an excellent tradeoff between Ron,sp and breakdown voltage [3-4]. GaN MOSFETs, on the other hand provide normally off operation, low gate leakage current, and large conduction band offset (3.6eV) making them less susceptible to hot electrons and other reliability issues [5].

Previously, n-channel GaN MOSFETs have been demonstrated on unintentionally doped (UID) and p-type GaN on Sapphire. These GaN MOSFETs exhibited high channel mobility (170 cm²/V-s), high breakdown voltage (940 V), and low interface state density (10¹⁰ /cm²-eV) [6-9]. In order to take advantage of the high mobility of the AlGaN/GaN HEMT’s 2DEG and reliability and high breakdown of the aforementioned MOSFETs, the MOS-HEMT concept was proposed. The MOS-HEMT effectively combines the two device structures allowing for a better Ron,sp vs. Breakdown tradeoff whilst maintaining reliability and enhancement mode behavior.

The MOS-HEMT is a MOS-gated device that functions in nearly the same fashion as a standard MOSFET, but has a drift region (region between channel and drain) made from an AlGaN/GaN heterostructure. The combination of an AlGaN/GaN HEMT and GaN MOSFET into a MOS-HEMT is shown in Figure 1.

![Fig.1 Cross section view of basic AlGaN/GaN HEMT, GaN MOSFET and how they combine to form a MOS-HEMT](image-url)
The theory and concepts behind the MOS-HEMTs operation are nearly identical to those for the MOSFET and HEMT on their own. It is a field effect device that modulates current flow between source and drain terminals via applied voltage to the gate terminal. The channel is formed at the surface of the GaN directly beneath the gate oxide just as it would be in a basic lateral GaN MOSFET. The major difference is that the regions between the source and channel, and channel and drain (drift region) are now a very high mobility 2DEG at the AlGaN/GaN interface rather than pure GaN. A basic MOS-HEMT that has been fabricated is shown in Figure 2; this device has experimentally demonstrated to have Ron,sp as low as 20mΩ-cm², a maximum field-effect mobility of 79 cm²/V-s, and a breakdown voltage of less than 200V due to dielectric breakdown [10]. MOS-HEMTs with breakdown voltages of 500V, and 1300V have been developed via more complex device structures that effectively reduce the field in the oxide to increase the breakdown voltage [11-12].

III. TECHNICAL RELEVANCE, IMPACT, AND APPLICATIONS

GaN based power devices provide a better Ron,sp vs. BV compared with Si and SiC power switching FETs; this is shown in Figure 3. The better tradeoff shows that it is possible to develop GaN transistors that will have less channel resistance at a given breakdown and thus less conduction loss when switching. The ultimate goal of GaN power device research is to replace Si based power FETs with GaN ones allowing for significant efficiency improvements for the various power electronics where Si power switching devices are used. The efficiency gained via GaN based power devices in turn yields more energy saving hybrid electric vehicles, dc-dc converters, inverters for solar and wind turbine applications, and any other high-voltage power electronic circuits.

![Fig. 2 Cross section view of lateral GaN MOS-HEMT](image)

![Fig. 3 Specific On-resistance vs. Breakdown Voltage for Si 4H-SiC, and GaN based FETs](image)
GaN devices are also able to operate in high temperature conditions where Si devices would not be functioning or reliable. The high temperature capabilities of GaN FETs allows for significant reduction in the size of heat sinks and cooling equipment that is currently necessary for Si based power electronics allowing for overall shrinking of the volume and weight of the power electronics. Additionally, GaN based devices are much smaller for a given breakdown voltage and current rating than the corresponding Si devices. These size and weight savings are of great importance in defense applications such as motor drives in fighter jets and ground vehicles where volume, weight, and power consumption are the most precious of commodities.

State of the art MOS-HEMTs have recently been shown to have improved $R_{on,sp}$ vs. BV characteristics via the use of high-k dielectrics. The use of ALD deposited Al$_2$O$_3$ as the gate oxide has enabled improved channel mobility and increased threshold voltage ($V_T$), and thus lower $R_{on,sp}$. The peak inversion layer mobility for the Al$_2$O$_3$ based MOS-HEMT is 225 cm$^2$/V-s [14-15]. Furthermore, since the dielectric constant of Al$_2$O$_3$ is greater than twice that of SiO$_2$ for a given gate voltage a MOS-HEMT made with a high-k gate will result in a larger inversion charge.

IV. EXPERIMENTAL PLAN

Recently, Professor Chow’s research group has designed and fabricated a device based on the basic MOS-HEMT structure, but optimized for improved breakdown voltage; the device is shown in Figure 4. In order to analyze the benefits gained via modifications to the basic MOS-HEMT structure seen in Figure 1, various device variations were included in the design. Devices were fabricated on UID and p-type GaN on Sapphire, variation to channel length, and drift length are design parameters varied in the fabricated devices. These design variations require characterization to demonstrate the tradeoffs between $R_{on,sp}$ and channel length, and breakdown voltage and drift length.

![Fig. 4 Cross section view of latest GaN MOS-HEMT fabricated by Professor Chow’s group.](image)

Additionally two different gate oxide deposition systems were used to determine which provides better field effect mobility for the MOS-gated region of the device. In order to properly characterize and analyze the aforementioned device design and process variations and compare with state of the art MOS-HEMTs and previous design cycles, it is necessary to test the devices and extract the following parameters:

- Specific on resistance vs. channel length and drift length via HP4155A Parameter Analyzer
- Breakdown voltage vs. channel length and drift length via HP4155A Parameter Analyzer
- Field effect mobility via HP4155A Parameter Analyzer
- MOS-gated Hall mobility via BioRad Hall effect system.

Additionally, it is worthwhile to study the effects of MOS channel scaling on $R_{on,sp}$ vs. breakdown voltage via simulations in MEDICI. Constant field scaling will be employed, and the investigation of Al$_2$O$_3$ as an alternative gate dielectric will also be explored. These simulations in conjunction with the data extracted from the new device lot characterization will help provide insight into optimization of the devices $R_{on,sp}$ vs. breakdown voltage, and the possibility of employing a new gate dielectric via atomic layer deposition (ALD) of Al$_2$O$_3$. 
V. EXPERIMENTAL & SIMULATED RESULTS

Unforeseen complications in the fabrication process caused the newly fabricated device lot to have a very poor yield. None of the short channel devices work due to issues in the deposition of the ohmic contacts. It is believed that the metal charge used during deposition was contaminated by metal flakes in the electron beam evaporator used to deposit the metal. Additionally it is believed that the metal was over etched rendering the smaller feature size devices useless. There were however long channel devices that could be characterized. With this being said, the processing problems resulted in a device lot from which characterization of $R_{on,sp}$ and breakdown voltage vs. channel length and drift length is impossible. However, since field effect mobility, $\mu_{FE}$, is most accurate when extracted from long channel devices, this portion of the experimental plan was able to be carried out. The MOS-gated Hall mobility characterization was not able to be done due to the small feature sizes of the Hall structure. The characterization of $\mu_{FE}$ permits the comparison of two gate oxide deposition systems. Once system is the AMAT P-5000 PECVD system at RPI, and the other is the same system, but at RIT. The two systems use the exact same recipe to deposit 100nm of PETEOS oxide for the MOS-HEMT’s gate dielectric. The output, transfer curves, and mobility curves for the 100μm channel MOS-HEMT using RIT deposited oxide are shown in Figure 5 (a)-(c), while Figure 6 (a)-(c) shows the same curves for the 100μm MOS-HEMT that uses RPI deposited oxide. The extracted data is summarized in Table 1.

![Device characteristics for 100μm channel MOS-HEMT with RIT deposited oxide.](image)

Fig. 5 Device characteristics for 100μm channel MOS-HEMT with RIT deposited oxide. (a) $I_{DS}$ vs. $V_{GS}$ with extrapolated $V_T=0V$, (b) output curve, (c) $\mu_{FE}$ vs $V_{GS}$ with a peak of 47cm²/V-s.
Fig. 6 Device characteristics for 100µm channel MOS-HEMT with RPI deposited oxide. (a) $I_{DS}$ vs. $V_{GS}$ with extrapolated $V_T = -3.6V$, (b) output curve, (c) $\mu FE$ vs. $V_{GS}$ with a peak of 20cm$^2$/V-s.

Table 1 Summary of extracted parameters for 100µm channel MOS-HEMTs comparing RIT and RPI gate oxide.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RIT Oxide</th>
<th>RPI Oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Voltage</td>
<td>0V</td>
<td>-3.6V</td>
</tr>
<tr>
<td>Field Effect Mobility</td>
<td>47cm$^2$/V-s</td>
<td>20cm$^2$/V-s</td>
</tr>
</tbody>
</table>

Figures 5 and 6, and Table 1 clearly indicate that the RIT oxide outperforms the RPI oxide, but is still not on par with the previously reported peak $\mu FE$ of 79cm$^2$/V-s. It should also be noted that neither of the devices are enhancement mode, a necessity for safe operation of any power device.

Despite being unable to experimentally characterize the effect of channel length and drift length on the $R_{on,ap}$ vs. BV relationship the effects of channel scaling on $R_{on,ap}$ were successfully simulated using MEDICI. Additionally channel scaling when a high-k gate dielectric is used was also investigated. The basic GaN material parameters as well a channel mobility of 79 cm$^2$/V-s, 2DEG mobility of 1500cm$^2$/V-s, velocity saturation $v_{sat}=2.5e7$ cm/s [14] are used create an accurate device model. Additionally the baseline structure has a drift length of 6.5µm and channel length of 6µm. The channel scaling process first explores the effect of only reducing the channel length from 6 to 0.5µm. Figure 7 shows $I_{DS}$ vs. $V_{GS}$, $V_T$ and $R_{on,ap}$ vs. channel length. It is clear that $R_{on,ap}$ decreases from 18.4 to 2.24mΩ·cm$^2$ indicating that channel scaling will definitely improve the $R_{on,ap}$ vs. BV tradeoff. Furthermore, as the channel length goes below 3 µm $V_T$ begins to fall rapidly indicating the onset of short channel effects, in particular drain induced barrier lowering (DIBL). Figure 8 gives further indication of DIBL as well as velocity saturation by showing non-saturating drain current and a reduction in the transconductance when the channel length goes from 1 to 0.5 µm. These effects are expected since constant field scaling was not employed.
Next constant field scaling was employed to permit the reduction in $R_{on,sp}$ without the accompanied short channel effects. The constant field scaling only actually scaled channel length and oxide thickness by a scaling factor $k$ because junction depth and doping are determined by the devices epitaxial structure and cannot be easily modified. The starting channel length is 3µm, and oxide thickness if 100nm, these values are then scaled by $k=1, 2, 4, 8$ resulting in a final channel length of .375 µm and oxide thickness of 12.5nm. The constant field scaling drastically reduced short channel effects while still decreasing $R_{on,sp}$ from 11.6 to 2.1 mΩ-cm². The scaling effect on $R_{on,sp}$ and suppression DIBL and velocity saturation are shown in Figure 9.

A more complex method that can be employed for reduction of short channel effects is the reduced surface field or RESURF concept. This is a widely used in power devices to improve the breakdown voltage while maintaining low $R_{on,sp}$. It is similar in theory to the lightly doped drain concept used in deep submicron CMOS devices. The RESURF concept is employed by introducing a1nm thick GaN cap layer to the device structure. The polarization charge in the capping layer will be opposite polarity to the fixed charges near the 2DEG and thus will balances some of those charges. This effectively reduces the electric field in the drift region and thus suppresses DIBL. Basic channel scaling (not constant field) simulations were performed on the GaN cap structure to demonstrate its effectiveness at suppressing DIBL.
Fig. 9 Effects of constant field scaling on $R_{on,sp}$, $I_{DSS}$ vs. $V_{GS}$ and transconductance. It is clear that $R_{on,sp}$ decreases while $V_T$ remains the same and transconductance continues to increase as channel length is scaled from 3 to 0.375 $\mu$m.

The channel is again scaled from 6 to 0.5 $\mu$m with all other dimensions remaining constant. The band structures in the MOS region for the 0.5 $\mu$m MOS-HEMT with and without the GaN cap biased at $V_{DS} = 25$ V, and $V_{GS} = 0$ V are shown in Figure 10 to demonstrate the existence of a barrier to electrons with the GaN cap and no barrier at all without implying that the RESURF concept implemented via the cap suppresses the effects of DIBL. This is confirmed by the saturating currents of the output curve as shown in Figure 11. The comparison of $R_{on,sp}$ vs. channel length for an AlGaN/GaN HEMT, MOS-HEMT, and MOS-HEMT with 1 nm GaN cap are also shown in Figure 11. The GaN cap structure has a slightly higher $R_{on,sp}$ because the polarization charge responsible for the DIBL suppression also depletes the 2DEG of some of its carriers making it more resistive.

Fig. 10 Comparison of band structure in the MOS region for 0.5 $\mu$m MOS-HEMTs with and without the 1 nm GaN cap layer. Devices are biases at $V_{DS} = 25$ V, $V_{GS} = 0$ V. DIBL is clearly depressed via GaN cap.
Finally channel scaling was employed comparing $\text{Al}_2\text{O}_3$ with $\text{SiO}_2$ as the gate dielectrics. The dielectric constant of $\text{Al}_2\text{O}_3$ is about 9 compared to 3.9 for $\text{SiO}_2$, so for a given capacitance the $\text{Al}_2\text{O}_3$ will be thicker than the $\text{SiO}_2$. Additionally, for the same electric field, a MOS capacitor using $\text{Al}_2\text{O}_3$ will achieve a greater than 2x increase in channel electron density. The model for the device using $\text{Al}_2\text{O}_3$ uses a channel mobility of 225$\text{cm}^2/\text{V-s}$ based on the state of the art devices mentioned in section III. Basic channel scaling was performed on the basic MOS-HEMT structure (no GaN cap) with 30nm thick $\text{Al}_2\text{O}_3$ and a device with 13nm thick $\text{SiO}_2$. The $\text{SiO}_2$ thickness was chosen such that the effective oxide thickness is the same for both structures. The channel length was scaled from 4 to 0.5$\mu\text{m}$. The resulting comparison of $R_{\text{on,sp}}$ vs. channel length is shown in Figure 12. It is clear that the $\text{Al}_2\text{O}_3$ based MOS-HEMT has much lower $R_{\text{on,sp}}$ which is expected since the channel mobility is larger.
VI. CONCLUSIONS

It has been shown that there is a discrepancy between MOS inversion layer mobility for MOS-HEMTs using PETEOS oxide from RIT vs. RPI. Additionally, the values extracted from this device lot are roughly half as large as previously fabricated MOS-HEMTs that show a peak $\mu_{FE} = 79 \text{ cm}^2\text{/V-s}$ which would still leave room for improvement. This low channel mobility will continue to rob the MOS-HEMT of its full potential as a power device with an outstanding $R_{on,sp}$ vs. BV tradeoff. In addition to the characterization results, it is apparent from the channel scaling and high-k gate dielectric MEDICI simulations that as channel length is reduced, $R_{on,sp}$ is also reduced. This implies that the key to overcoming the mobility problems in AlGaN/GaN based MOS gated devices is to scale the channel length as drastically as possible while maintaining long channel behavior. It is also paramount to experimentally investigate the use of high-k gate dielectrics, in particular Al$_2$O$_3$ as a means to increase the MOS channel mobility and to prevent short channel effects. Figure 13 provides a summary of the channel scaling effects on $R_{on,sp}$ vs. BV for GaN MOS-HEMTs using SiO$_2$ gate dielectric, AlGaN/GaN HEMTs, and silicon based power devices.

![Fig. 13 Summary of $R_{on,sp}$ vs. BV for medium and short channel GaN MOS-HEMTs, HEMTs, and silicon based power devices.](image-url)

VII. CONTINUING CHALLENGES & FUTURE WORK

In order to harness the full potential of GaN based FETs for power switching circuits it is paramount that the fabrication process be optimized and refined to provide highly reproducible devices with a high yield. Advanced processing techniques are also critical to viably producing complex MOS-HEMT structures. In particular the discrepancies in channel mobility between the RIT and RPI PETEOS oxides needs to be understood. Before any other work goes into the design of new MOS-HEMT structures, the mobility needs to be increased at least back up to 79cm$^2$/V-s, and higher if at all possible. Additional work includes the fabrication of sub-micron MOS-HEMTs using both SiO$_2$ and Al$_2$O$_3$ oxides for the gate stacks. This should be done to confirm the simulation results for channel scaling and the effect of high-k dielectrics on the operation of the AlGaN/GaN MOS-HEMT.
REFERENCES


