

HETERODIMENSIONAL FIELD EFFECT TRANSISTORS FOR ULTRA LOW POWER APPLICATIONS

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Abstract—We describe a new class of field effect transistors (FETs) based on a heterodimensional contact between a three-dimensional gate (metal or semiconductor) and a two-dimensional electron gas. The heterodimensional FET family (2D MESFET, 2DI MESFET, and 2D JFET) has shown significant promise for future high speed, ultra low power applications. We review the recent developments, and report on a new fully ion implanted quasi-heterodimensional FET, the Coax-2D JFET.

Index terms—Heterodimensional FET, Low Power.

I. INTRODUCTION

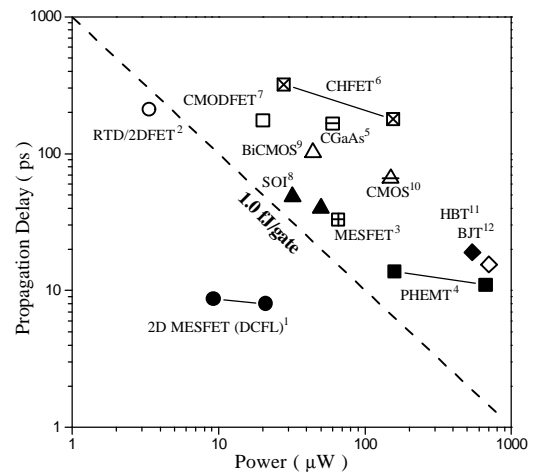
New technological advances have to be made at the device, circuit, and system level in order to meet increasing demands for high speed, low power digital integrated circuits (ICs).¹⁻² This is particularly important for battery powered applications such as wireless communications and portable computing. However, it is becoming increasingly more difficult to decrease the power-delay product below the 1.0 fJ/gate range due to limitations in the physics of conventional devices (see Fig. 1).

In this paper, we discuss a fundamentally new device technology based on heterodimensional contacts between three-dimensional (3D) gate (metal or semiconductor) and two-dimensional electron gas (2-DEG).³⁻⁷

The term “heterodimensional” refers to a contact between semiconductor regions of different dimensions, such as a sidewall metal gate contacting the edge of a thin conducting layer in an epitaxially grown heterostructure (Fig. 2). Such contacts have unique electronic and geometric properties which provide a larger depletion width, smaller capacitance, higher breakdown voltage, and superior electron confinement compared to conventional semiconductor device structures,³⁻⁷ and an enhancement of Schottky barrier height of the metal gate contact.⁸ In addition, the narrow gate effect, which leads to parasitic currents at the gate edges in a top-gated structure, is eliminated by the novel side gate geometry.⁶ Thus, it allows for deep submicron scaling of both the gate length and channel width of heterodimensional Field Effect Transistors (HD-FETs). Together, the electronic and geometric properties of these devices offer exciting

potential for innovative applications in millimeter wave,^{3,9-10} optoelectronic,¹¹ and low power electronic circuits.^{6,12}

One example of these devices is a 2D MESFET (Fig. 2). The 2D MESFET utilizes the 3D Schottky metal/2-DEG junction to laterally modulate the current flowing between drain and



Circles -Heterodimensional Device (AlGaAs/InGaAs/GaAs) **Triangles** -Si devices
Squares -GaAs-based devices **Diamonds** -SiGe devices

Fig. 1. Power-delay chart for different technologies representative of the state-of-the-art; (1) Peatman, et al, *Proc. DRC*, 1995; (2) Robertson, et al, *Proc. ISDRS*, 1995; (3) Vitesse Semiconductor Corp.; (4) Suehiro, et al, *IEEE TED*, 1994; (5) Hallmark, et al, *ISSSE*, 1995; (6) Baca, et al, *Proc. GaAs IC Sym.*, 1994; (7) Yoh and Harris, *Proc. IEDM*, 1987; (8) Shahidi, et al, *Int'l Conf. on Solid State Dev. and Mat.*, 1994; (9) Taft and Hayden, *IEEE EDL*, 1995; (10) Sadek, et al, *IEEE TED*, 1996; (11) F. Sato, et al, *Proc. IEDM*, 1992; (12) S. Marksteiner, et al, *Micro. Eng.*, 1992. Points (1), (2), (3), and (10) are simulated while the other values are experimentally measured.

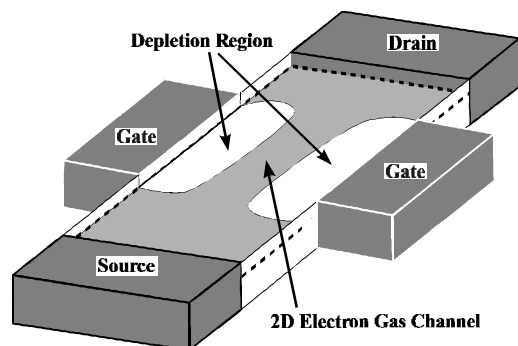


Fig. 2. Bird's eye view of the 2D MESFET. Sidewall Schottky gates modulate the 2-DEG channel.

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source. As shown in Fig. 1, this new technology may substantially reduce the power-delay product.

These HD-FETs in particular, the 2D MEFET,⁵⁻⁶ 2DI MEFET,¹³ and 2D JFET¹⁴ have shown significant promise for future high speed, ultra low power applications, where large bandwidth, greatly increased energy efficiency, and dramatically smaller device dimensions will be required. In this paper, we describe the HD-FET family, and the device fabrication and performance. We also report on a fully ion implanted, quasi-heterodimensional FET, the “Coax-2D JFET”, using a fully manufacturable process.

II. DEVICE DESIGN AND FABRICATION

A. Heterodimensional Contacts and Fabrication

Figure 3 shows the different types of heterodimensional contacts, and the evolution toward a more manufacturable process.

The key step in the fabrication of any heterodimensional device is the formation of the sidewall gates. Typically, this is accomplished by an etch-and-plate process. In such a process, the gate pattern is first formed lithographically, either via ultra violet or electron beam technology. Next, a trench is formed by etching through the 2-DEG down to the buffer layer. Finally, the gate metal is plated in the trench via an electrochemical process. This basic process has been applied to several different devices, including the Schottky metal/2-DEG diode,³ the 2D MEFET,⁵⁻⁶ and the Schottky-gated resonant tunneling transistor (SG RTT).¹⁰

In above devices, the heterodimensional contact occurs between the electroplated Schottky gate and the 2-DEG channel provided by a GaAs-based heterostructure, e.g., the AlGaAs/InGaAs/GaAs heterostructure (Fig. 3 (a)).

The second type HD-FET is the 2DI MEFET (2D Implanted-channel MEFET), where the 2-DEG is replaced by a thin Si-ion-implanted channel in a bulk GaAs wafer

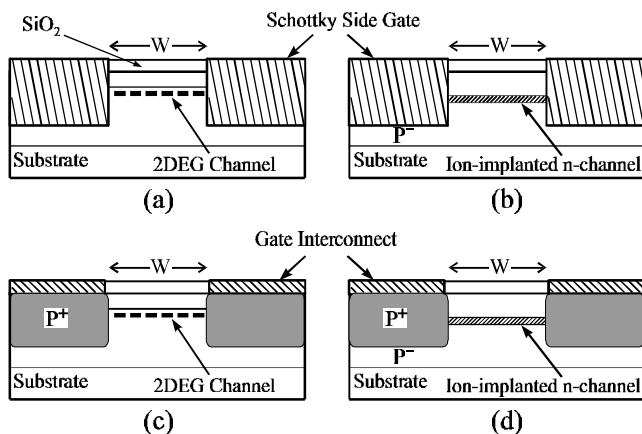


Fig. 3. Cross-section of 4-type heterodimensional contacts in HD-FETs: (a) 3D metal/2-DEG (2D MEFET), (b) 3D metal/ion-implant channel (2DI MEFET), (c) 3D p-region/2-DEG, and (d) 3D/2D p-n junction (2D JFET).

(Fig. 3 (b)). The ion-implanted process is more compatible with commercial GaAs IC fabrication.

The 2DI MEFETs have excellent electrical characteristics at sub-half-micron channel widths, including low output conductance, low saturation voltage, and large ON/OFF ratio.¹³ However, the 2DI MEFET process still faces a major manufacturability roadblock — the sidewall Schottky contacts formed by the electrochemical plating are not generally used in the production of commercial GaAs ICs. An alternate method for obtaining the basic geometry of the 2D MEFET is to replace the etch/plate Schottky gate process with p⁺ implants (Fig. 3(c)). Then a fully ion implanted, quasi-heterodimensional field effect transistor, the 2D JFET, becomes possible (Fig. 3 (d)). The 2D JFET, fabricated on bulk n-GaAs, utilizes p⁺ Be implants on either side of a very thin Si-implant ($7 \times 10^{12} \text{ cm}^{-2}$ at 40 keV) to laterally modulate the conducting channel between the source and drain.

B. HD-FET Design

Figure 4 shows examples of the HD-FET device design. Figure 4 (a) represents the classic HD-FET design, where the 3D Schottky dual gates may be either electrically tied together or biased independently. For logic operations, the ability to bias the dual side gates independently is an advantage, which allows for an increase in the logic functionality of 2D MEFET low-power logic circuits.¹⁵ In order to increase the logic functionality further, more gates can be added as shown in Fig. 4 (b). A NOR operation using a dual-gate 2D MEFET and a NAND operation using a triple-gate 2D MEFET have been demonstrated, where resonant tunneling diodes were used as the load devices.^{15,16}

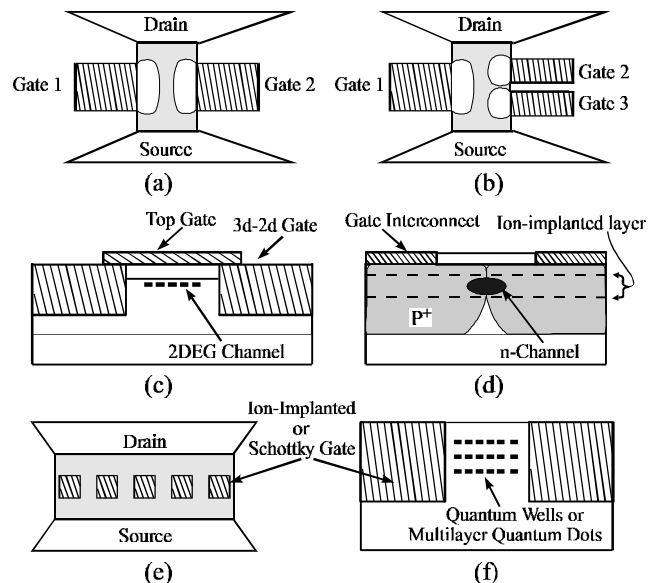


Fig. 4. Device designs - 6 type HD-FETs: (a) dual-gate, (b) triple-gate, (c) quasi-coaxial gate, (d) “Coax” gate (or all-around gate), (e) multiple-gate (multi-channel type I), and (f) multi-quantum wells (multi-channel type II), or multi-layer of quantum dots.

When a top gate is added, the channel will be confined by Schottky gates on three sides (Fig. 4 (c)). This “quasi-coaxial” MESFET should have better sub-threshold characteristic for low power IC applications.¹² In principle, this top Schottky gate can be added in all the HD-FETs shown in Fig. 3.

An all-around gate FET (real “Coax-2D FET”) would be the best choice for a further better confinement; hence for better sub-threshold characteristic for ultra low power IC application. One such design is illustrated in Fig. 4 (d), which is similar to Fig. 3 (d). The key parameters of the fabrication process are the activation (or diffusion) temperature and time of the implant p^+ regions. The p^+ implants must diffuse from both p^+ regions to the center to form an all-round p-n junction. In principle, in order to provide a better confinement, a heterostructure barrier or a buried p-type layer can be placed under the n-channel in the quasi-coaxial FET (Fig. 4 (c)), and in all the structures shown in Fig. 3 if they have a top gate.

For microwave applications, a multiple channel device having 48 parallel 0.5- μm channels has been fabricated on a double delta-doped $\text{Al}_{0.24}\text{Ga}_{0.76}\text{As}/\text{In}_{0.18}\text{Ga}_{0.82}\text{As}/\text{GaAs}$ heterostructure.⁹ The multi-channel 2D MESFET, as sketched in Fig. 4 (e), offers higher current capabilities as well as an improved impedance matching at microwave frequencies compared to a single channel 2D MESFET.

Compared with multi-channel structure in Fig. 4 (e), the structure in Fig. 4 (f) offers (1) a higher power and more controllable fabrication for a microwave power amplifier using the multi-quantum wells (QWs), and (2) a higher quantum efficiency for the photoelectronic detector when using the QWs or the multi-layer quantum dots. It is also a useful structure for the investigation of quantum effects in low dimensional electronic systems, which can be tuned by the gate bias. The side Schottky gates can be also replaced by ion implanted regions as discussed above. In fact, a novel heterodimensional laser - $\text{GaAs}/\text{InGaAs}$ lateral injection ridge laser,¹⁷ has been demonstrated using a similar structure, where a p-implanted “gate” on one side, and a n-implanted “gate” on another side contact the QWs. This lateral current injection laser is inherently more suitable for planar opto-electronic ICs, and frees the vertical dimension for control of laser operation and for novel functionality.

III. DEVICE PERFORMANCE

The DC and RF characteristics of selected prototype heterodimensional devices are shown in Fig. 5 and 6.

The electrical characteristics of the 0.5x0.5 μm 2D MESFET and 2DI MEFSET are nearly identical as shown in Fig. 5 (a) and (b).⁵ However, the ion-implanted device does not require MBE growth and is therefore cheaper to manufacture.

Fig. 5 (c) shows the measured drain current characteristics of a Coax-2D JFET having nominal gate length and width of

1x1 μm . Following the RTA, the effective gate width becomes $\sim 0.5 \mu\text{m}$. The threshold voltage of this device is 0.1 V, the peak current at $V_{\text{gs}}=0.5 \text{ V}$ is 10 μA , and the saturation voltage at $V_{\text{gs}}=0.5 \text{ V}$ is 0.35 V. As evident from the figure, the output conductance is negligible (less than 0.5 mS/mm) despite the narrow channel width.

The prototype multiple channel 2D MESFET having 48 parallel 0.5- μm channels has been tested using an HP 8510C network analyzer.⁹ The f_T and f_{max} of the device were measured to be 14 GHz and 45 GHz, respectively. The current gain-frequency characteristics are shown in Fig. 5 (d). Higher cutoff frequencies should be possible with further optimization of the device.

As shown in Fig. 5, the first three prototype devices exhibit a very small drain current, a small saturation voltage, a flat saturation drain current and a near-zero threshold voltage.

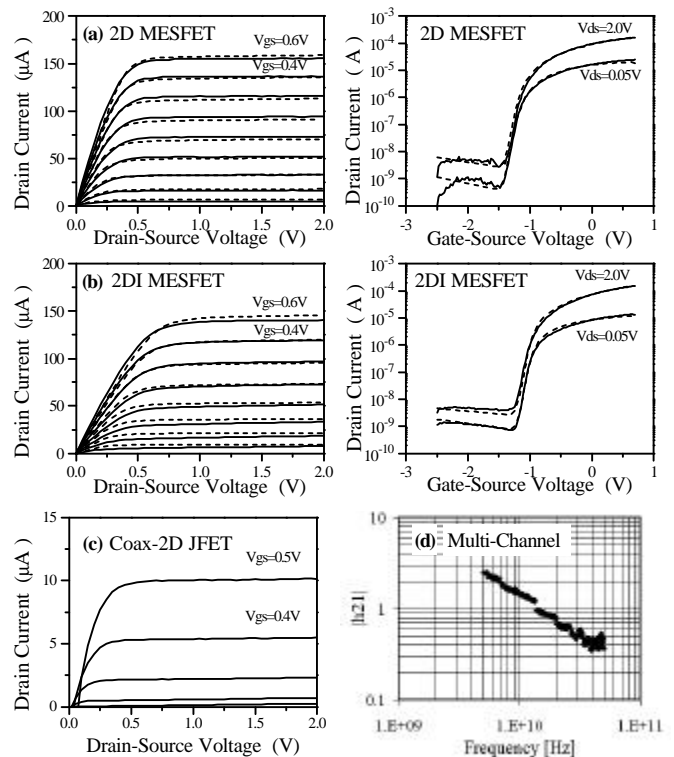


Fig. 5. The DC and RF performances of selected prototype HD-FETs. The dashed lines are modeled using AIM-Spice.

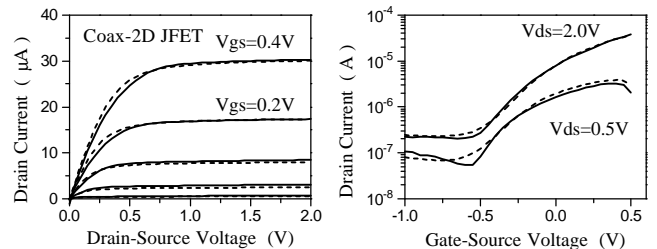


Fig. 6. Measured (solid) and modeled (dashed) drain current characteristics of a Coax-2D FET. The gate length is 4 μm and the width is 2 μm . The leakage current should improve by at least one order-of-magnitude following optimization of the isolation etch and the gate metal.

The results for the multiple channel devices suggest that the HD-FET is suitable for operation in microwave region. Along with the features as mentioned in Section I, this shows significant promise for future high speed, ultra low power digital, analog and mixed IC applications.

In parallel with the progress in the device design, fabrication and testing, the device and circuit models have been developed and implemented in the circuit simulator AIMSpice.^{5-6,12,16,18-20} The simulation examples are shown in Fig. 5 (a) and (b), and Fig. 6, where the dashed lines represent simulated results.

IV. CONCLUSION

We have described the progress in the design, fabrication, testing, and modeling of the heterodimensional field effect transistors. The heterodimensional technology used in this new class of FETs offers many novel features, and can eliminate the narrow channel effect. The recently fabricated fully-ion-implanted 2D JFET offers excellent low power characteristics using a fully manufacturable process and is very promising for future ultra-low power IC applications.

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