A novel via-first, back-end-of-the-line (BEOL) compatible, monolithic wafer-level three-dimensional (3D) integration technology platform is being developed, which employs wafer bonding of damascene-patterned metal/adhesive redistribution layers on two wafers, thus facilitating both high density of inter-wafer electrical interconnects and strong adhesive bond of two wafers in one unit processing step. Two key steps for this approach are 1) fabrication of a metal/adhesive redistribution layer on the top of the BEOL-processed wafer by damascene patterning and 2) face-to-face alignment and bonding of two wafers utilizing the metal/adhesive redistribution layers. Repeating a whole 3D process flow, the third wafer (or more) can then be added. Copper/tantalum (Cu/Ta) and Benzocyclobutene (BCB) are selected as the metal and adhesive for the feasibility demonstration of the via-first 3D approach. Critical processing challenges are investigated, including 1) BCB partial curing and patterning; 2) Ta and Cu deposition; 3) Cu/BCB chemical mechanical planarization (CMP); 4) post-CMP treatment; and 5) bonding process parameters.

Wet chemical and dry plasma surface preparation techniques are used for post-CMP treatment and pre-bonding surface preparation, a critical step in facilitating a strong, reliable bond between BCB-to-BCB regions as well as a low contact resistance between Cu-to-Cu regions. Results on blanket BCB/Si wafers show a strong BCB-to-BCB bond with mean critical adhesion energy in a range of 14-31 J/m². For patterned Cu/BCB wafers, interfaces of bonded BCB-to-BCB, Cu-to-Cu, and BCB-to-Cu areas are imaged by focused ion beam scanning electron microscopy (FIB/SEM), showing the feasibility of these bonds. Specific contact resistance of the Cu-to-Cu interconnect is on the order of 1x10⁻⁷ Ω·cm², a promising preliminary result indicating electrical contact is possible using this new 3D technology platform.

Introduction

Three-dimensional (3D) integration technology holds promise for reducing interconnect delays in future integrated circuits (ICs) by reducing length and number of long interconnect lines [1-3] as well as offering heterogeneous integration of processes and devices through die-to-die, die-to-wafer, or wafer-to-wafer approaches [4-6]. Of these approaches, monolithic wafer-level processing also holds promise for decreasing cost through parallel fabrication methods for high volume manufacturing. Various wafer-level approaches have been demonstrated [1-3], with each approach having its own advantages. For example, the dielectric bonding technology platform offers a robust bonding process [1], the handle wafer process offers simple alignment capability [2], and the copper bonding technology platform offers a means for simple electrical interconnect [3]. For the integration of fully fabricated wafers in a packaging facility, the capabilities offered by both the dielectric bonding and copper bonding approaches are clearly critical. Furthermore, the ability to easily fabricate a general redistribution layer for routing of signals between generic ICs is also needed.

This paper introduces, for the first time, a novel via-first, back-end-of-the-line (BEOL) compatible, monolithic wafer-level 3D integration technology platform, which employs wafer bonding of damascene-patterned metal/adhesive redistribution layers on two wafers, thus providing inter-wafer electrical interconnects (via-first) and adhesive bonding of two wafers in one unit processing step. A conceptual schematic of the via-first approach is illustrated in Figure 1. Copper/tantalum (Cu/Ta) and Benzocyclobutene (BCB) are selected as the metal and adhesive for the feasibility demonstration of this via-first 3D approach. This diagram shows a damascene patterned Cu/BCB redistribution layer over the uppermost metal layer of a second substrate, which is then inverted, aligned, and bonded to another patterned Cu/BCB layer on the first substrate. The substrate of the face-down bonded second wafer is then thinned. The process can be extended to multiple wafer stacks by etching through the thinned top layer of the bonded pair to create another damascene patterned redistribution layer which mates with a third substrate.
This via-first approach using wafer bonding of damascene-patterned metal/adhesive redistribution layers provides: 1) both electrical and mechanical inter-wafer connections/bonds (combining advantages of both BCB/BCB and Cu/Cu bonding); 2) thermal management options: Cu/BCB “redistribution layer” can serve as a good thermal conductor/spreader (with large percentage of Cu area), or as a good thermal insulator (with large percentage of BCB area), or selected area for any kind; 3) possibility for high inter-wafer interconnect density while allowing large alignment tolerance by eliminating deep inter-wafer vias; and 4) a “redistribution layer” as inter-wafer interconnect routing for wafers, on which the inter-wafer interconnect pads are not matched. This approach is attractive for applications of monolithic wafer-level 3D integration (e.g., 3D interconnect, 3D ICs, wireless, and smart imagers, etc.) as well as wafer-level packaging, passives, mechanical-electrical microsystems (MEMS), optical MEMS, bio-MEMS, and sensors.

Clearly, the bonding process for such a technology platform would be challenging, as a variety of surfaces are exposed including the dielectric adhesives, diffusion barriers, and electrical conductors. Ideally, all should be capable of being bonded to one another without interfering with the electrical characteristics of the Cu-to-Cu interconnection. Surface preparation techniques for improving adhesion of BCB to silicon and silicon nitride [7] as well as copper [8] have been discussed in the literature, but not with respect to a wafer bonding application. Further, wafer bonding of soft baked BCB has been well documented for the 3D application [9-10], as has damascene patterning of copper in fully cured BCB [11-12]. Here, we propose that a partially cured BCB layer should offer the best compromise between patterning capability and bond quality. This work aims to qualify the needs for this material set in this bonding application.

**Experimental**

Bonding of two single level copper damascene processed wafers with BCB inter-layer dielectric (ILD) was chosen for the demonstration of the via-first 3D approach. For this demonstration, partially cured BCB is explored for use as a bonding layer. Dow AP3000 adhesion promoter is spun onto oxidized 200 nm silicon wafers prior to coating with Cyclotene 3022 dry-etch formulation BCB. These films are partially cured on a 250°C hotplate under a nitrogen purge for 60 seconds. Post cure BCB thickness is measured to be about 1.1 microns using reflectance spectrometry. BCB films are patterned using 0.9 micron thick AZ7209 photoresist in an i-line stepper. The BCB is then etched in an inductively coupled plasma etcher. Etching parameters were held constant for each wafer: source RF power was 1500 W, substrate RF power was 500 W, $\text{C}_4\text{F}_8$ flow was 60 sccm, $\text{O}_2$ flow was 180 sccm, pressure was 12.5 mTorr, temperature was 0°C, substrate distance from the plasma source was 200 mm. These parameters resulted in a bias voltage of about 470 V. This process produces approximately a 1:1 selectivity of BCB to photoresist, and a BCB etch rate of about 250 nm/min. The BCB is etched through the entire film thickness, thus the photoresist is assumed to be entirely consumed during etching.

Tantalum and copper are then sputtered over the patterned BCB; Ta sputtering is performed at 500 W, resulting in a sputter rate of about 12 nm/min, and copper is sputtered at 1700 W, resulting in a film deposition rate of about 70 nm/min. These sputter power levels are reduced from the standard power levels to suppress further curing of the partially cured BCB, and are similar to values reported in previous work [13].

A baseline two-stage CMP process employing commercially available two-component (abrasive and oxidizer) slurries is utilized to polish the copper and tantalum. For the first stage copper removal EKC Microplanar 9001 (abrasive) and 9007 (oxidizer) are used, and for the second stage tantalum removal EKC Microplanar 9003 (abrasive) and 9011 (oxidizer) are used. This second stage slurry is formulated to be highly tantalum selective over copper. A Rodel IC1400 k-groove pad is used, with the pad conditioned in deionized water using the manufacturers standard diamond grid for an IPEC 372M polisher. The conditioning process parameters were kept constant: 20 rpm conditioner and platen rotation, arm pressure of 0.2 PSI, for a duration of 30 seconds before each wafer was polished. CMP process parameters were also held fixed for all wafers and included a 5.0 psi arm pressure, 0.5 psi back pressure, 90 rpm platen rotation, 90 rpm carrier rotation, and slurry flow of 200 ml/min for the copper removal. The Ta CMP process differed in that the arm pressure was 2.5 psi, pad and carrier rotation were 75 rpm, and the slurry flow was 175 ml/min. Wafers were polished for several minutes at a time, and visually inspected to determine endpoint. Post-CMP double-sided brush cleaning was performed on all wafers using Rippey PVA brushes in deionized water in a two-stage process.

These damascene patterned films are aligned and bonded under controlled vacuum, temperature, and pressure parameters. Two bond processes were investigated: one involved temperature ramp to 250°C under 10,000 N bonding force for one hour, while another added a second ramp to 350°C under the same pressure for one hour. The latter explores the possibility for stacking multiple wafers using a 250°C partially-cured BCB-to-BCB bond for structural support, and using a higher temperature anneal (350-400°C) to promote copper-to-copper bonding as a final step.

After bonding, these pairs underwent a three-step thinning process. The top silicon wafer was thinned to ~100 microns thickness by grinding and polishing at Aptek, with final thinning in tetramethyl ammonium hydroxide (TMAH). For a via-chain structure, the top silicon is completely removed for convenience, stopping on the oxide layer. This three-step thinning process has been reported elsewhere [14], and has proven to be particularly useful for demonstrating the viability of wafer pairs for 3D integration [1].

At this point the wafer was broken to allow a lot split for 1) cross-sectional imaging and 2) electrical characterization. Cross-sectional imaging was done using a Zeiss Crossbeam FIB/SEM. Due to the nonconductive nature of the majority of the area imaged, charging was suppressed by coating the top surface with palladium. Cross-sectional areas were then milled quickly in an auto-cut mode, followed by polishing slowly using an 8 nm to 10 nm step size to allow fine features...
to be imaged. For electrical characterization, the top silicon dioxide and tantalum layers are removed in an O$_2$ + CHF$_3$ (1:10 ratio) reactive ion etch at 150 W. With these layers removed, contact can be made to the top copper surface. A probe station with 0.5 to 1 micron size probe tips was used to scratch the copper surfaces and make electrical contact to the via-chain structures to determine the specific contact resistance.

To further explore a critical point in this process, a variety of surface preparation techniques are employed between the fabrication of the redistribution layer and the wafer-to-wafer bonding step. These process steps need to serve as a post-CMP clean and be capable of preparing both the BCB and copper surfaces for bonding. For this study, BCB films are spun and partially cured in the baseline process, then subjected to the baseline second stage CMP process for 60 seconds. The post CMP clean / bonding preparation techniques explored include: 1) two stage, double sided brush cleaning with deionized water (our baseline post CMP clean), 2) baseline brush cleaning followed by vacuum dehydration bake, 3) baseline brush cleaning, sulfuric acid dip, water rinse, and vacuum dehydration bake, and 4) baseline brush cleaning, vacuum dehydration bake, and nitrogen plasma surface activation.

Four-point bending is employed to identify any differences in the resulting bonding critical adhesion energy as a result of these processes [9]. For this technique, several beam specimens are cut from the bonded wafer pairs with a nominal 4 mm by 40 mm geometry. Edges are polished, and a pre-crack is formed using a silicon dicing saw which cuts through the top wafer to within about 20 microns of the bonding layer. These samples are then chemically etched in TMAH at a temperature of 95°C for 30 minutes to propagate the pre-crack to the bonding interface. This chemical treatment etches silicon in a highly selective fashion over BCB. The samples are then placed in a material testing jig on the four-point bending tool as described elsewhere [9-10]. Load deflection curves were obtained using several recipes; parameters were modified slightly in an effort to obtain consistently flat plateau regions for calculation of adhesion energy. Best results were obtained with a loading deflection rate of 2 µm/min, followed by a delamination region which triggered on a 2 N drop in measured force and used a deflection rate of 0.5 microns/min for 60 min, followed by a hold step for 15 minutes. Many acceptable load-deflection curves were obtained with a recipe that simply employed a constant 2 µm/min deflection rate throughout the process.

**Results and Discussion**

Damascene-patterned wafers are used for inspection of the bonding interfaces (i.e., BCB/BCB, Cu/Cu and Cu/BCB bonds) and electrical characterization of the Cu/Cu bond. Blanket BCB/Si wafers are used for evaluation of various surface preparation techniques to facilitate strong bonds.

FIB/SEM was used to obtain cross sectional views of the bonding interfaces in a bonded pair. One resulting image from the characterization of the 350°C bonded wafer pair is shown in Figure 2. Both BCB-to-BCB interfaces and copper-to-copper interfaces are almost seamless, indicative of good

![Figure 2: FIB/SEM cross-section showing bonding interfaces; (A) Region A showing two grain boundaries crossing original copper-to-copper interface; (B) Region B showing BCB-to-BCB, BCB-to-tantalum, and BCB-to-copper interfaces. Photo taken by Art Dewey, Carl Zeiss SMT Inc.](image-url)
bonding, although bonding across the wafer needs to be further investigated. Furthermore, a grain boundary crossing the original copper-to-copper bond interface is indicated in Region (A). Previously published results [15] indicate that a temperature greater than 300°C is required to achieve lower than 1% die failure during dicing of Cu-Cu bonded structures, and that an interface free bond is achievable when bonding and annealing temperatures are greater than 350°C and 90 min respectively. Another area of interest is the void at the BCB/Ta/Cu interface, as indicated by Region (B), which shows that the copper-to-BCB interface is not well bonded with the Cu surface that is not well planarized. However, BCB does not flow into the void in Region B, indicating that the copper-to-copper bond will not be contaminated by the BCB processing when CMP provides the level of planarization requisite for this process. The copper-to-copper fusion bonding and no BCB reflow are clearly confirmed in Figure 3. While the process used may not be ideal for obtaining good copper-to-BCB adhesion, we believe that demonstrating feasibility of BCB-to-BCB bonding and copper-to-copper bonding in a single unit process is an important first step in realizing this technology platform.

Electrical data was taken on a bonded pair of single level damascene wafers by removing the top oxide in a standard RIE process. Via resistance across several vias with copper-to-copper connection is measured, although large via-chains were not achievable with the via-chain structure used. An optical micrograph shown in Figure 4 illustrates the via-chain for specific contact resistance measurements on the wafers bonded at 350°C. Top metal structures are easily discernable from bottom metal structures in an optical microscope because the tantalum layer is on top of the copper structure in this case. After removal of the SiO2 in RIE, a layer of polymer, which is easily penetrated by the electrical probes, is seen over the top metal. Copper-to-copper contact is clearly visible from Figures 2 to 4. This contact area was measured by optical microscopy to be on the order of 1x10^{-7} cm² for the structures tested. For the 350°C bonded wafer, resistance was measured to be in the range of several ohms across devices with multiple layer-to-layer copper interconnects, when the contact resistance of the probes was subtracted out. Thus specific contact resistance is on the order of 1x10^{-7} Ω·cm². Bonded copper-to-copper specific contact resistance has been reported elsewhere [16] and this preliminary data on the first batch of patterned, 350°C bonded wafers from this process shows that the specific contact resistance is one to two orders of magnitude higher than for 400°C bonded wafers from [16].

Four-point bending was used to quantify the critical adhesion energy of partially cured BCB bonded silicon wafers under a variety of surface preparation conditions [9,10]. Important geometric parameters are identified in Figure 5, and Equation 1 is used for all critical adhesion energy calculations.

\[
G_i = \frac{3(1-\nu_s^2)p_i^2h^3}{2E_J^i h^3} \left[ \frac{1}{\eta_i^2} - \lambda \left( \eta_i^2 + \lambda \eta_s^2 + 3\lambda \eta_i \eta_s \right) \right] (\text{Eq. 1})
\]

Where \( \lambda \) is the effective modulus equal to \( E_d(1-\nu_s^2) / E_i(1-\nu_i^2) \), \( p_i \) is the saturation load, \( l \) is the spacing between the inner and outer loading pins, \( b \) is the specimen width, and \( n_i \) is the relative height of the top and bottom bonded silicon, \( n_i = h_i/h(i=1,2) \). A typical load-deflection curve for tests in this study is illustrated in Figure 6.

![Figure 3: FIB/SEM cross-section. Point A: Cu void on top wafer is filled by Cu from bottom wafer, indicating Cu fusion bonding; Point B: Cu void on bottom wafer is not filled by BCB, indicating no BCB reflow, thus minimizing possible Cu bond contamination by BCB.](image)

![Figure 4: Example optical micrograph of via chain for specific contact resistance measurements. Small pads are 6 μm by 6 μm, large pad is 10 μm by 10 μm. Three copper-to-copper interconnections are measurable in this chain.](image)

![Figure 5: Beam specimen geometry for four point bending.](image)
Table 1 details the material parameters and critical adhesion energy values obtained through four-point bending for the various experimental conditions on blanket BCB/Si wafers. The value shown for soft baked BCB (~35% cured) is taken from previously published results [1,9-10] and is shown for comparison. The one-sigma error for the value shown using this well-developed baseline soft baked BCB bonding process was commonly less than 10% of the average value. While the values presented for partially cured BCB in this via-first process are still in development, it is reasonable that the added processing steps between the BCB deposition and the bonding process contribute to the increase in spread in adhesion energy values.

Of the surface preparation techniques explored here, only the nitrogen plasma activation technique shows marked decrease in adhesion energy. This technique is explored because of the reported improved adhesion between copper and BCB [7-8]. This data suggests that a tradeoff may exist between BCB-to-BCB and BCB-to-copper adhesion energies using this surface preparation technique. The load deflection curves for this set of samples, as illustrated in Figure 7, clearly showed more fluctuation in the measurement than the other sample sets did; particulate contamination introduced in the process is a possible explanation.

During four-point bending, delamination occurs at the weakest interface; in all cases except the nitrogen plasma treated case, the vast majority of delamination is at the silicon/adhesion promoter/BCB interface, rather than BCB-to-BCB interface. This can easily be inspected visually, and is confirmed by reflectance spectroscopy. In only about half of the specimens tested, very small areas of BCB can be observed on the silicon surface; the thickness of this BCB is measured to be 1.1 µm, equal to the original BCB thickness. For the nitrogen plasma treated case, delamination is observed at the BCB-to-BCB interface, and BCB of the original thickness is measured on both broken surfaces after four-point bending. Since the majority of the delamination is not at the BCB-to-BCB interface, the critical adhesion energy for partially cured BCB-to-BCB bonding should be similar to that of soft-baked BCB, therefore providing similar wafer bond strength.
Summary and Conclusions

Feasibility of wafer bonding of metal/adhesive redistribution layers on two wafers, for the first time to our knowledge, is demonstrated for a novel via-first, BEOL compatible, monolithic wafer-level 3D integration technology platform. Specifically in this work, a copper damascene patterning process has been used to form a planarized redistribution layer in partially cured BCB on 200 mm wafers, and both copper and BCB surfaces are successfully bonded in a single unit process under controlled temperature and pressure conditions. Preliminary data from structures fabricated with this platform show a bond strength comparable to previously reported BCB dielectric bonding, as well as promising electrical inter-wafer Cu interconnection characteristics. With the very promising results obtained to date, the remaining critical processing challenges will be further investigated.

This via-first approach to 3D integration combines the advantages of dielectric adhesive bonding, which is a robust bonding process and provides high wafer bond strength, with pre-bonding inter-wafer copper interconnects for process integration simplicity. It also provides thermal management options as well as possibility for high inter-wafer interconnect density. The metal/adhesive redistribution layer can also serve as inter-wafer interconnect routing for bonded wafers.

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References