Via-First Inter-Wafer Vertical Interconnects utilizing Wafer-Bonding of Damascene-Patterned Metal/Adhesive Redistribution Layers

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ABSTRACT

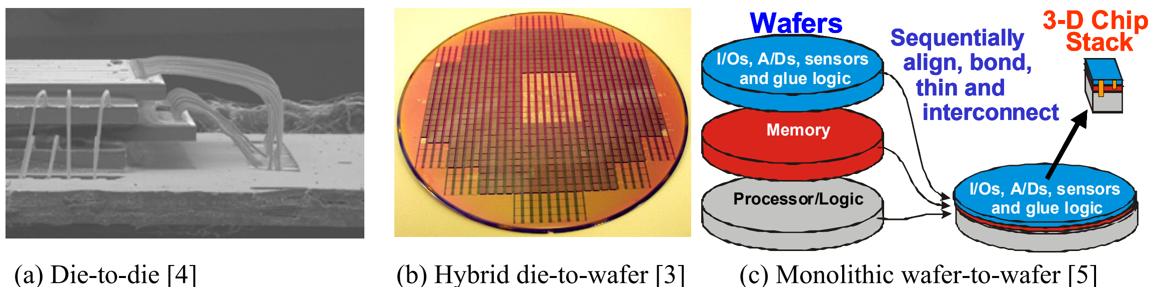
Three-dimensional (3D) integration with through-die vias offer improved electrical performance compared to edge-connected wire bonds in stacked-die assemblies. Monolithic wafer-level 3D integration offers the potential for a high density of micron-sized through-die vias necessary for highest performance of integrated systems. In addition, such wafer-level technologies offer the potential of lowest cost in large manufacturing volume of any heterogeneous integration platform, incorporating the inherent low cost of monolithic IC interconnectivity. After a brief summary of current 3D integration technologies, a recently introduced platform that offers the process integration advantage of copper-to-copper (Cu-to-Cu) bonding with the increased adhesion strength and robustness of dielectric adhesive bonding using benzocyclobutene (BCB) is discussed. Critical processing challenges of the new platform include BCB partial curing compatible with damascene patterning, post-damascene-patterning cleaning and surface activation, bonding process parameters, and wafer-level planarization requirements. The inherent incorporation of a redistribution layer into the bonding layer process further reduces the process flow and is compatible with wafer-level packaging (WLP) technologies.

3D IC TECHNOLOGIES

Three major 3D IC approaches being pursued are: 1) die-to-die, 2) hybrid die-to-wafer, and 3) monolithic wafer-to-wafer 3D integrations, as shown in Fig. 1. Die-to-die approach or vertical multi-chip packaging is in current use [1]. The other two major approaches have the potential for higher interconnect density, higher performance capability and lower cost for high-throughput production [2]. Die-to-die 3D integration is not discussed further in this paper.

Both die-to-wafer and wafer-to-wafer approaches are expected to yield better performance than conventional chip-to-chip or multi-chip packaging integration due to lower parasitics (both RC delay and inductance), because of shorter inter-chip connections. Both approaches also allow the integration of sub-blocks within circuits for added design flexibility and optimization capability due to denser inter-chip interconnectivity, while maintaining the separation of incompatible processes on different wafers. However, there are significant differences between these two approaches.

The die-to-wafer approach offers the use of known-good-die (KGD) [3], and the assembly flexibility allows high yield for products in low-to-medium quantities. This approach has a higher cost compared to monolithic wafer-to-wafer approaches for large production volumes, since alignment and bonding is done by "pick-and-place" assembly process; i.e., in die-by-die fashion. While die yield issues need to be considered further, smaller die and wafer-specific processing indicate that yield may not be a limiting factor with a robust monolithic wafer-level 3D process.



(a) Die-to-die [4] (b) Hybrid die-to-wafer [3] (c) Monolithic wafer-to-wafer [5]

Figure 1. Three major 3D IC approaches.

Moreover, the monolithic wafer-to-wafer approaches have many performance advantages, such as a very high density of low parasitic inter-chip interconnects for high bandwidth and increased noise immunity. Most important, lower high-volume interconnect cost should be possible with monolithic wafer-level processes.

Wafer-level 3D IC technologies are being actively pursued because of these advantages. The 3D IC approaches based on wafer bonding and inter-wafer interconnects generally involve four major processing steps: 1) wafer-to-wafer alignment, 2) wafer-to-wafer bonding, 3) wafer thinning, and 4) inter-wafer interconnection. Fig. 2 shows a schematic of wafer-level 3D integration [5].

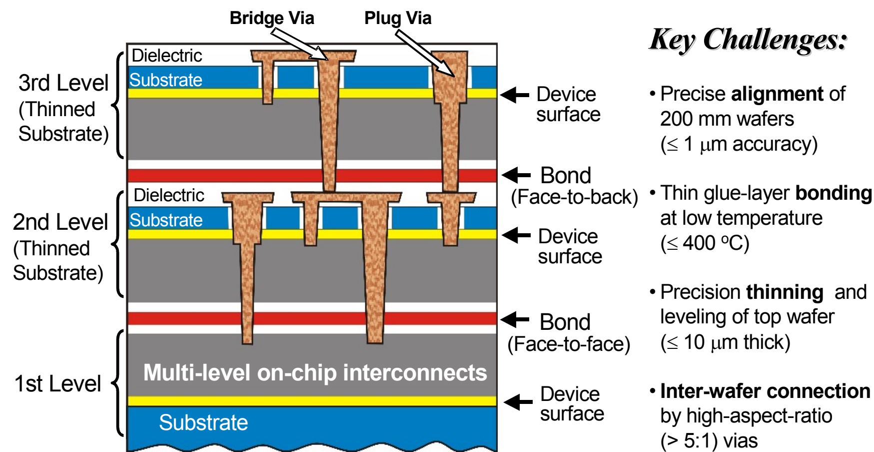


Figure 2. Schematic of a monolithic 3D hyper-integration concept using adhesive wafer bonding and copper damascene inter-wafer interconnects, showing bonding interface, vertical inter-chip vias (plug- and bridge-type), and "face-to-face" and "face-to-back" bonding [5].

Approaches to inter-wafer interconnection include copper damascene patterning, tungsten fill and etch-back, and through wafer fill using either polysilicon or metal. Wafer alignment and thinning techniques vary and are application specific. While not yet demonstrated as production-ready, no technology show-stoppers have been delineated to date.

Planarization can be particularly important for 3D IC technologies because most 3D IC approaches involve an intimate wafer-to-wafer bonding process [5]. Since the bonding process follows significant on-wafer processing (all front-end and some or all back-end interconnect), wafer planarity is more difficult to achieve than for silicon-on-insulator (SOI) technologies involving wafer bonding. Feature-scale, die-scale and wafer-scale planarity requirements are considered specifically severe for metal-to-metal bonding with previously processed vertical interconnect structures.

In terms of wafer bonding, three major approaches are under investigation, as shown in Fig. 3:

1) Direct oxide bonding at low temperature, where inter-wafer interconnects are formed after wafer bonding and thinning (i.e., a via-last 3D approach) [6]. Direct oxide bonding for 3D IC applications requires compatibility with back-end-of-the-line (BEOL) processes, such as low bonding pressure and low bonding and post-bonding anneal temperature. This bonding approach is sensitive to particulates and requires damage-free atomic scale surface planarization in addition to the desirable surface activation.
2) Metal-to-metal bonding, where metal bonds also serve as inter-wafer interconnects (i.e., a via-first 3D approach). The bonding material candidates include copper [7], solder [8] or micro-bump [9] with or without underfill. Issues with surface oxidation, interface contamination, and particularly the surface non-planarity may causes micro-voids, thereby impacting the inter-wafer interconnect yield and reliability. Use of solder or other alloy for the metal-to-metal bonding may alleviate the stringent bonding surface requirement; however, compatibility with subsequent metallization and packaging processing as well as next-wafer level 3D processing would likely be compromised or limited. This approach has been demonstrated for two or more wafers in the 3D "wafer-stack" [10].
3) Dielectric adhesive bonding, where inter-wafer interconnects are formed by high-aspect-ratio (HAR) vias through the thinned top wafer and the bonding adhesive into the top of the multilevel on-chip interconnect of

the bottom wafer (i.e., a via-last 3D approach) [5]. These adhesives can be curable polymers, polyimides or other adhesives. Key advantages with this approach include the ability to accommodate wafer-level non-planarity (e.g., surface topography, wafer bow) and particulates at the bonding interfaces; high bond strength; relative low temperature bonding process as well as high temperature stability after bonding discussed in the following sections. Depending on the adhesive properties, 3D ICs with more than two wafers are possible.

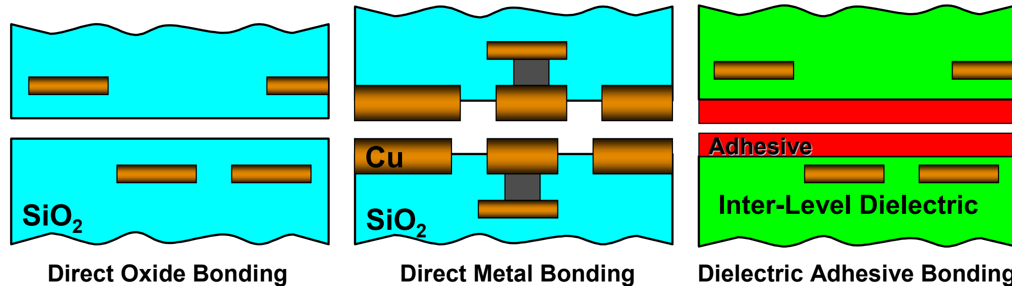


Figure 3. Three major bonding approaches for wafer-level 3D ICs. Common issues include BEOL IC process compatibility, planarization and interface activation, wafer thinning and leveling without edge chipping, wafer-to-wafer alignment approach and inter-wafer interconnection methodology.

This paper focuses on a new wafer-level 3D approach to via-first inter-wafer vertical interconnects utilizing wafer-bonding of damascene-patterned metal/adhesive redistribution layers, which combines the electrical and process integration advantages of direct copper-to-copper inter-wafer interconnect bonding, the thermal-mechanical advantages of BCB adhesive wafer bonding, and the wafer-level packaging advantages of the inter-wafer redistribution layer technology.

VIA-FIRST 3D PLATFORM WITH BONDING OF METAL/ADHESIVE REDISTRIBUTION LAYERS

A recently introduced via-first 3D technology platform [11] currently under investigation employs wafer bonding of damascene-patterned metal/adhesive redistribution layers on two wafers, thus providing inter-wafer electrical interconnects (via-first) and adhesive bonding of two wafers in one unit processing step. A conceptual schematic of the via-first approach is illustrated in Fig. 4. Copper/tantalum (Cu/Ta) and Benzocyclobutene (BCB) are selected as the metal and adhesive for the feasibility demonstration of this via-first 3D approach. This diagram shows a damascene patterned Cu/BCB redistribution layer over the uppermost metal layer of a second wafer, which is then flipped, aligned, and bonded to another patterned Cu/BCB layer on the first wafer. Note that the patterned Cu/BCB layer on the first wafer can also be a Cu/BCB redistribution layer if needed (not shown in Fig. 4). The substrate of the face-down bonded second wafer is then thinned. The process can be extended to multiple wafer stacks by etching through the thinned second wafer of the bonded pair to create another damascene patterned layer, which mates with a third wafer. Note that the patterned Cu/BCB layer on the thinned second wafer substrate can also be a Cu/BCB redistribution layer if needed (not shown in Fig. 4). Moreover, an extra Cu/oxide redistribution layer can be added prior to any Cu/BCB layer patterning process (e.g., over the uppermost metal layer of the third wafer as shown in Fig. 4), thus to simplify the Cu/BCB patterning process because only Cu bonding posts (vias) are needed. This latter approach offers also simple bonding scheme, i.e., with minimum misalignment one is always bonding Cu posts to Cu posts and BCB field to BCB field, avoiding undesirable contact (i.e., bonding) of long Cu lines with BCB field (see the bonding layers between second and third wafers as shown Fig. 4); most importantly, this approach provides much more redistribution capability than that combining Cu bonding vias with the redistribution layer (e.g., the Cu/BCB redistribution layer on front side of the second wafer as shown in Fig. 4).

This via-first approach using wafer bonding of damascene-patterned metal/adhesive redistribution layers provides: (1) both electrical and mechanical inter-wafer connections/bonds (combining advantages of both BCB/BCB and Cu/Cu bonding); (2) thermal management options: Cu/BCB "redistribution layer" can serve as a thermal conductor and/or spreader (with large percentage of Cu area), or as a thermal insulator (with large percentage of BCB area), or selected area for any kind; (3) high inter-wafer interconnectivity while allowing large alignment tolerance by eliminating deep inter-wafer vias; and (4) a "redistribution layer" as inter-wafer interconnect routing for wafers, on which the inter-wafer interconnect pads are not matched, which further reduces the process flow and is compatible with wafer-level packaging (WLP) technologies. This approach is attractive for applications of monolithic wafer-

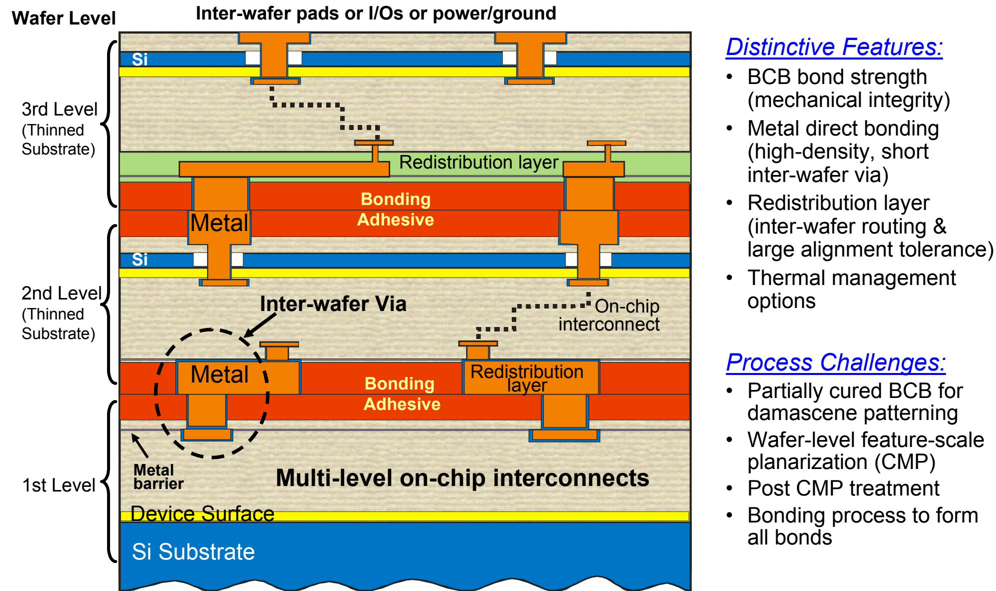


Figure 4. Schematic of Cu/BCB redistribution layer bonding for via-first 3D integration (Cu-Cu bonds provide inter-wafer interconnects and BCB-BCB adhesive bonds provide mechanical wafer attachment).

level 3D integration (e.g., 3D interconnect, 3D ICs, wireless, and smart imagers, etc.) as well as wafer-level packaging, passives, mechanical-electrical micro-systems (MEMS), optical MEMS, bio-MEMS, and sensors.

Clearly, the bonding process for such a technology platform would be challenging, as a variety of surfaces are exposed including the dielectric adhesives, diffusion barriers, and electrical conductors. Ideally, all should be capable of being bonded to one another without interfering with the electrical characteristics of the Cu-to-Cu interconnection. Surface preparation techniques for improving adhesion of BCB to silicon and silicon nitride as well as copper have been discussed in the literature, but not with respect to a wafer bonding application. Further, wafer bonding of soft baked BCB has been well documented for the 3D application [5], as has damascene patterning of copper in fully cured BCB [12]. Here, we propose that a partially cured BCB layer should offer the best compromise between patterning capability and bond quality.

Fabrication of resistive via chains using the via-first redistribution layer approach, which has been reported previously [11], is summarized here. A 2 μm thick thermal oxide was grown on 200 mm silicon wafers. BCB was then spun onto these substrates to a nominal thickness of 1.2 μm, and partially cured in a coat/bake track modified to include a nitrogen purge. The BCB partial cure temperature was 250°C and hold time was 60 seconds, resulting in ~55% BCB crosslink. The partially cured BCB was photolithographically patterned in an i-line stepper, and then etched in an inductively coupled plasma (ICP) etcher using C_4F_8 and oxygen as reactive species. Tantalum liner and copper were sputtered over the patterned BCB at power levels suitable for deposition over a polymer dielectric. Chemical-mechanical planarization (CMP) was carried out on this film stack using commercially available slurries and pads until the pattern was well defined. Post CMP brush cleaning was done with deionized water and PVA brushes. These single-level damascene patterned redistribution layers were then aligned and subsequently bonded in a vacuum chamber. The bond process included a mechanical downforce of 10,000 N, and a temperature ramp to 250°C and soak for 60 minutes, followed by a further ramp to 350°C and soak for 60 minutes and cooling to room temperature. The bonded pair was thinned to a nominal thickness of 50 μm through grinding and polishing, followed by a wet chemical etch in tetramethyl ammonium hydroxide (TMAH), which has high Si-to-SiO_2 selectivity, to completely remove the remaining silicon.

After the above fabrication procedure, the bonded pair was sectioned, allowing a lot split for characterization of structural and electrical properties. For the structural characterization, a cross-sectional focused ion beam / scanning electron microscopy (FIB/SEM) was used with a thin Pt layer deposited on the wafer as a grounding layer. One

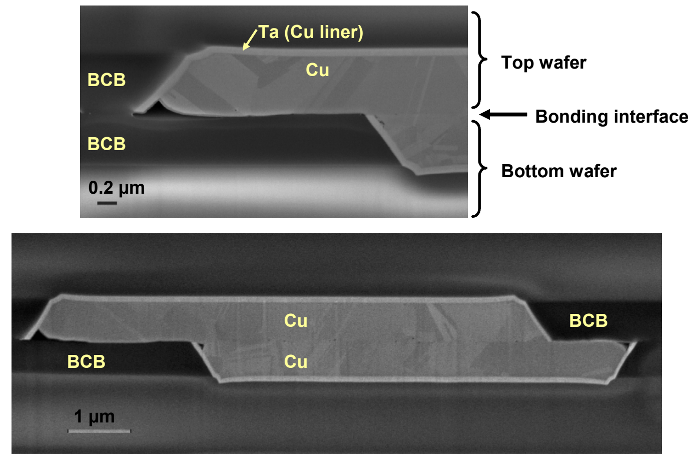


Figure 5. Cross-sectional FIB/SEM image of bonded damascene patterned Cu/BCB wafers showing well bonded Cu-to-Cu, BCB-to-BCB interfaces [11].

resulting cross-section of the bonded area near the wafer center is depicted in Fig. 5. This figure shows a bonded Cu-to-Cu interface, a bonded BCB-to-BCB interface, and a Cu-to-BCB interface that appears to be in intimate contact, but not well-bonded. For the electrical characterization, the surface oxide (originally the isolation layer under the copper/BCB redistribution layer) is removed to allow access to the via-chains. A two-point probing setup was used to measure electrical resistance on several inter-wafer vias, and optical microscopy was used to measure the overlap area. Resulting contact resistance was found to be on the order of 1×10^{-7} Ω–cm^2.

Planarization of damascene patterned Cu/BCB redistribution layers at feature, die, and wafer length scales is critical because wafer scale effects such as TTV, and wafer level variation of feature-scale planarity can significantly affect alignment tolerance, bonding yield (percentage of bonded area), and chipping at the edge of the wafers during thinning. Features at two differing locations on the 200 mm damascene patterned wafer are shown in Fig. 6; one feature is in a die near the center of the wafer and the other feature is in a die at the edge of the wafer. The copper features are slightly raised with respect to the BCB surface: ~60 nm for the centrally located die and ~120 nm for die near the wafer edge. Since Cu/BCB patterns are bonded near the wafer center as shown in Fig. 5, while they are not well bonded near the wafer edge, the authors believe that feature scale nonplanarity should be controlled to at better than 100 nm over the entire wafer to optimize bond yield [13]. Further research is needed to better quantify the allowable feature-scale nonplanarity as well as wafer-scale nonplanarity.

The results shown in Figs. 5 and 6 are quite promising, demonstrating the feasibility of this new via-first 3D approach. Initial results also show a bond strength more than half of the BCB-BCB bond strength established in previous research (> 15 J/m^2 compared to 32 J/m^2), which is more than a factor of 3 greater than needed with damascene-patterned IC interconnects (5 J/m^2). However, key challenges still need to be overcome and are currently under investigation. These challenges include (1) optimization of the BCB partially-curing process, thus to provide sufficient bond strength and serve as a damascene patterning-compatible dielectric material for Cu/BCB redistribution layer material, (2) characterization of wafer-level feature-scale planarity of the Cu/BCB redistribution layer fabricated by single-level chemical-mechanical planarization (CMP) technique, (3) post-CMP surface treatment and wafer bonding schemes to facilitate the bonds of Cu-to-Cu, BCB-to-BCB and Cu-to-BCB over the entire wafer in one unit process step, (4) low resistivity of electrical inter-wafer Cu interconnection, and (5) redistribution layer design and fabrication schemes.

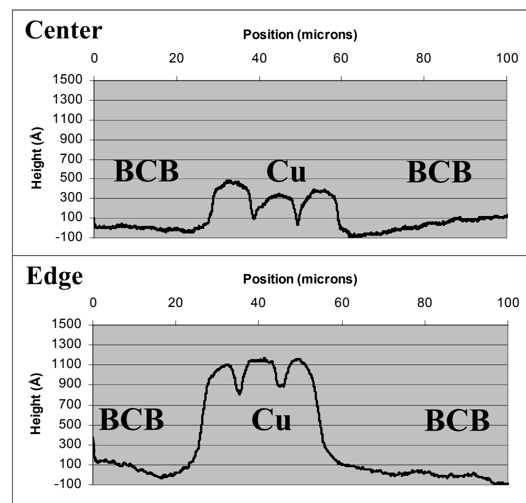


Figure 6. Feature level nonplanarity for structure in centrally located die versus structure in die near the edge of 200 mm wafer [13].

SUMMARY AND CONCLUSIONS

While die-to-die stacked packages using thinned die offers optimal form factor in products today and through-die vias with tens of microns diameter offer a promising technology in the near term, wafer-level 3D integration with micron-sized through-die connectivity offers the highest inter-wafer interconnect density, low electrical parasitics and lowest manufacturing cost in high-quantity manufacturing. A via-first 3D platform for inter-wafer vertical interconnects utilizing wafer-bonding of damascene-patterned metal/adhesive redistribution layers has been presented that has the high bonding strength of dielectric adhesive bonding, the direct inter-wafer interconnects with Cu-to-Cu bonding, and thermal design flexibility, while incorporating an inter-strata redistribution layer within the bonding layer.

Key issues with the realization of this platform include BCB partial curing compatible with Cu damascene patterning, post-CMP cleaning and surface activation prior to alignment and bonding, bonding process parameters (particularly thermal budget) and wafer-level planarization requirements. While excellent BCB-to-BCB bond interfaces and promising Cu-to-Cu interface properties (some grain growth and reasonable contact resistivity with 350°C maximum processing temperature), incomplete bonding is observed at the Cu-BCB bonding interface, with process nonuniformities across 200 mm-diameter wafers.

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