Who invented 3D integration?

Recently I found a blog called “Who Invented the Through Silicon Via (TSV) and When?” where it noted that in 1958, the Nobel laureate William Shockley filed a corresponding patent introducing through semiconductor vias - calling them “deep pits.” Indeed, Shockley was involved in the first realization of a transistor, but it should be mentioned that a transistor concept was already patented in 1925 by Julius Edgar Lilienfeld. So, who invented the transistor? Correspondingly, one explicit inventor of 3D integration cannot be manifested — and of course, 3D integration is much more than the drilling and filling of TSVs ...

On the other hand, a few pioneering teams involved in the realization of 3D integration can certainly be named. The concept of 3D IC was claimed in 1964 by R.W. Haisty, R.E. Johnson and E.W. Mehal of Texas Instruments Inc., and the patent of through connections for connecting circuits on both sides of the semiconductor wafer was filed in 1964 by M. Smith and E. Stern of IBM. In 1969, M. Koyanagi and colleagues at Tohoku University demonstrated 3D IC integration by wafer bonding. Corresponding die-to-wafer stacking technologies for KGDs, which are significant for 3D integration of heterogeneous systems, were developed by Fraunhofer Munich (patents filed in 1994 by P. Ramm and R. Buchner). And certainly you can call the author of the following article, James Jian-Qiang Lu from Rensselaer, one of the inventors of 3D integration: Since the late 1990s, in fact, he has made distinctive contributions in this research area, with more than 150 publications covering 3D integration platforms, technologies and design. I am proud to say that James Lu, together with Philip Garrou and me, authored the overview chapter “Three-Dimensional Integration” in the recently published “Handbook of Wafer Bonding” (Wiley). One of his articles, “3D Integration: Why, What, Who, When?” can be found in Future Fab International, Issue 23 (2007).

James Lu’s article in the following section represents an outstanding overview on this emerging technology in the past five decades, as well as showing the current developments toward commercialization.

Abstract

Three-dimensional (3D) hyper-integration has recently been recognized as an emerging technology to lead to an industry paradigm shift due to its tremendous benefits. The concepts of 3D integrated circuits were conceived almost five decades ago. Worldwide academic and industrial research and development were actively conducted in the last decade; products and prototypes toward volume production have been demonstrated. Wide adoption still faces major technical and business challenges, but it holds a promising future for smart-systems applications.

Introduction

3D integration is an emerging technology that vertically stacks and interconnects multiple materials, technologies and functional components to form highly integrated micro-nano systems. This is expected to lead to an industry paradigm shift due to its tremendous benefits in performance, data bandwidth, functionality, heterogeneous integration and power.

3D integration is currently seen as the leading candidate to extend the benefits of Moore’s Law to future IC technology nodes and to provide “More than Moore” solutions in the post-CMOS era (Figure 1). By means of stacking and connecting function blocks vertically, 3D technology can overcome some physical, technological and economic limits encountered in planar ICs to extend Moore’s Law life. The most critical component in 3D integration is the through strata via (TSV) or through silicon via (TSV); a massive number of short TSVs can electrically connect multiple strata of ICs and/or devices vertically, enabling high performance, high functionality, compact heterogeneous systems with high data bandwidth and speed, and low power consumption and manufacturing cost.

This article attempts to briefly review some important developments in the past five decades, as well as provide some perspective on 3D hyper-integration for future smart systems. It is by no means comprehensive, but hopefully it will shed some light on the research and development of 3D hyper-integration. Critiques and comments are welcome.

3D Integration: Past and Present

With the technology development of 3D integration in the past five decades, we may consider roughly four periods of time:

• 1960s to 1970s: Generation of 3D integration concepts
• 1980s to early 1990s: First wave of 3D technology research
• Late 1990s to 2000s: Second wave of 3D technology R&D toward commercialization
• 2010s to future: Third wave of 3D technology for smart systems

**Generation of 3D Integration Concepts**

3D is not new. We have always been living in a 3D world. Humans have created 3D buildings for thousands of years. Electrons were created in 3D in their early stages. Not long after the first integrated circuit (IC) was invented by Jack Kilby in 1958, the 3D integration idea was conceived. Evidence can be found from the following patents:

- R.W. Haisty et al. (Texas Instruments Inc.), “Three-Dimensional Integrated Circuits and Methods of Making Same,” U.S. Patent No. 3,613,226, filed on Aug. 18, 1964 and granted on Oct. 19, 1971. A continuation of the application originally filed in 1964 was filed in 1971 with the same inventors and same patent title; the patent was granted on July 24, 1973 with U.S. Patent No. 3,748,548.


The last two patents described 3D integration technologies closer to present practices. A number of technical papers were published in this period of time. Some research efforts on 3D integration technology and circuit design were documented in two books:


However, it seems that it was a failed practice, without any commercially viable 3D products in the market in this period of time. The author believed that the major reason for this failed practice was a lack of demand and supporting technologies. It was a wonderful time period for 2D-IC commercial products, following Moore’s Law of exponential growth in IC chips for computer technology, leading to the revolution of information technology.

**First Wave of 3D Technology Research**

Active 3D integration research started in early 1980s, with more patents and technical papers published.  


- M. Yasumoto, et al. (NEC, Japan), “Process of Fabricating Three-Dimensional Semiconductor Device,” U.S. Patent No. 4,612,083, filed on July 17, 1985 and granted on Sept. 16, 1986. In this patent, no TSV was needed.

- M.J. Little and J. Grinberg (Hughes Aircraft Company), “3-D Integrated Circuit Assembly Employing Discrete Chips,” U.S. Patent No. 5,032,896, filed on Aug. 31, 1989 and granted on July 15, 1991. In this patent and its related publications, the thermmigration of aluminum through silicon to form signal paths through silicon wafers was used and further developed.

- Y. Tomita, et al. (Matsushita Electric Industrial Co.), “Three-Dimensional Stacked LSI,” U.S. Patent No. 5,191,405, filed on Nov. 19, 1989 and granted on Mar. 2, 1993. In this patent, the interlayer via-hole wiring to power IC was introduced.


**Second Wave of 3D Technology R&D Toward Commercialization**

In 1997, IBM announced its six-level copper interconnect technology, which opened a new chapter of interconnect technology for improving IC performance.

In 1998, a multi-university research center, Interconnect Focus Center (IFC), was created, with major funding from
Semiconductor Research Corporation (SRC) and the U.S. Defense Advanced Research Projects Agency (DARPA). The overarching goal was “to discover and invent new interconnect solutions that will meet or exceed ITRS projections.” Major contributing universities in IFC were Georgia Institute of Technology (GIT), University of Albany (UA), Massachusetts Institute of Technology (MIT), Rensselaer Polytechnic Institute (RPI) and Stanford University. Thanks to the leadership and vision of the center director, Prof. J.D. Meindl, 3D integration was established as the IFC Flagship program.[1-4] Also, thanks to Profs. A. Kaloyeros, UA and RPI received significant funding from the New York State Office of Science, Technology and Academic Research (NYSTAR, now “New York State Division of Science, Technology and Innovation”) for 3D integration research. Many aspects of 3D integration design and technologies were investigated and reported directly to major semiconductor companies and in a number of journals and international conferences. The research outcomes from the IFC 3D programs planted the seed for the second wave of 3D integration technology.[1-4]

The major driving force was “interconnect limits on performance of gigascale integration (GSI),” where demand to “go vertical” results from the need to drastically reduce the long interconnects on 2D chips. The second important reason 3D integration could become a successful practice is that it became feasible to develop the four key 3D technologies: wafer alignment, wafer bonding, wafer thinning and inter-strata interconnect, because they had been actively researched and developed for micro-electro-mechanical systems (MEMS) in the 1990s.

In 2003, Dr. D.J. Rada in DARPA created the first major 3D IC program (DARPA BAA 03-25, Three Dimensional Integrated Circuits); articulated a clear technology vision based on 3D heterogeneous integration; recruited the best researchers from universities, national labs and semiconductor companies; and formed a new 3D research community. The legacy of this successful program resulted in DARPA funding several other large 3D programs. Results from these efforts have greatly contributed to a wider understanding of 3D integration and 3D infrastructure development.

A number of academic institutions, industrial consortia and semiconductor companies across the globe started research and development in 3D integration. Results were reported in journals, conferences and books.[1, 5-8] More patents were applied and granted. A set of critical 3D processes and equipment for alignment, bonding, thinning and inter-strata interconnection (such as TSVs) were developed.[1, 5-7]

Since TSV became the heart of 3D integration recently, it is worth mentioning some of the development (to the author’s knowledge) as follows:
- The term “TSV” was used for the first time by Prof. L. Schaper and his student in their paper presented in the IMAPS International Conference on Advanced Packaging and Systems (ICAPS). Reno, Nevada, March 11, 2002.[9]

The term TSV was widely accepted, probably after Dr. K. Lee (Samsung Electronics) presented his world-first, eight-NAND stack functional sample at the 3rd International Conference of 3-D Architectures for Semiconductor Integration and Packaging in November 2006, and Dr. C.-G. Hwang (president and CEO of Samsung Electronics) gave his keynote of “New Paradigms in the Silicon Industry” at the IEEE International Electron Devices Meeting (IEDM) in December 2006.

3D-TSV R&D and Business
Currently we are moving into the third wave of 3D integration. 3D-TSV technology has been actively developed by a number of academic institutions, government labs, industrial consortia and semiconductor companies around the world. Several corresponding full-3D processing flows have been demonstrated, with a number of approaches investigated. Particularly, after the use of TSVs for image sensors, TSV technology is getting into prime time for TSV silicon interposers (e.g., Xilinx’s giant FPGAs), wide I/O applications (e.g., 3D DRAMs) and heterogeneous products for low-power, high-performance and small-factor smart-system integration.

Infrastructures (equipment, ECAD tools and standards) are being rapidly established. Several consortia are working with semiconductor companies to develop 3D- TSV technologies and define ecosystems.

3D Hyper-Integration Perspectives
With a number of companies announcing their timelines and roadmaps for 3D products, the focus of research and development turns to thermal-mechanical-electrical reliability of 3D TSV integrated systems, and the design of 3D systems with particular consideration of thermal issues.

Development of 3D integration will move from chip-on-chip (CoC) platforms to chip-on-wafer (CoW) platforms. Cu TSV technology in particular is close to maturity and is gaining up for volume production of wide I/O 3D DRAMs and for giant FPGAs with TSV Si-interposers, while image sensors using TSVs have been in the market for a few years. Once the infrastructure and ecosystem are in place, 3D IC technology development and applications will continue advancing in the coming years in an evolutionary, instead of revolutionary, fashion, from CoC to CoW and wafer-on-wafer (WoW) platforms (Figures 1 and 2). The author believes that a good set of solutions for processing integration, thermal-mechanical stress, yield and test, as well as cost reduction, will be developed for 3D hyper-integration of future smart systems for computing, information technology, mobile and mixed-signal applications, biomedical devices, and power and smart lighting applications.

3D hyper-integration provides a viable path to a future paradigm combining powerful computer technology with many applications, so that future smart systems can easily interact with people and the environment. Such systems can be smart information/communication systems (for cloud computing, handheld devices, wireless communications, etc.), smart-sensing control systems (for automobile transportation, avionic system, drones, etc.), future LED-based smart-lighting and new energy systems, smart biomedical systems (for diagnosis, surgery, drug delivery, health sensing/monitor, or brain-computer interfaces (BCIs), etc.), just to name a few. The future promises to be an exciting time. Our daily lifestyle and even our
culture may be dramatically changed with proliferation of this 3D hyper-integration technology.

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References


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James Jian-Qiang Lu is an IEEE fellow and an IMAPS fellow and life member. He has been working on 3D hyper-integration technology since the late 1990s at Rensselaer Polytechnic Institute in the Electrical, Computer and Systems Engineering department. James has more than 200 publications in the micro/nano-electronics area from theory and design to materials, processing, devices, integration and packaging. His particular interest is 3D hyper-integration of smart systems.