3D Integration: Why, What, Who, When?

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Abstract

Three-dimensional (3D) integration is an emerging technology that is expected to lead to an *industry paradigm shift* due to its tremendous benefits. Worldwide academic and industrial research activities currently focus on technology innovations, simulation and design, and product prototypes. Anticipated applications start with memory, portable device and high-performance computers and extend to high-density multifunctional heterogeneous integration of infotech-nanotech-biotech systems.

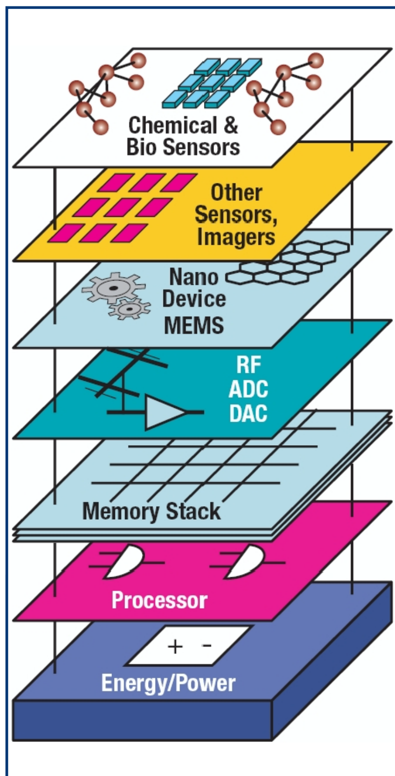

Figure 1. A vision of future 3D hyper-integration of infotech, nanotech and biotech systems – a new paradigm for future technologies.

Introduction

Three-dimensional (3D) integration is an emerging technology that can form highly integrated systems by vertically stacking and connecting various materials, technologies and functional components together, as shown in Figure 1. The potential benefits of 3D integration can vary depending on approach; they include multifunctionality, increased performance, reduced power, small form factor, reduced packaging, increased yield and reliability, flexible heterogeneous integration and reduced overall costs. For example, a small form factor is achieved by stacking active component layers on top of one another in any 3D approach. Speaking at the 2006 IEEE International Electron Devices Meeting (IEDM), Dr. Chang-Gyu Hwang, president and CEO of Samsung Electronics, stated that "*…rapid adoption of 3-D integration technology seems to be essential and, thankfully, unavoidable.*" He believes that the industry paradigm will shift to a new industry-fusing technology era that will offer tremendous global opportunities for expanded use of 3D silicon-based technologies in highly integrated systems. Indeed, 3D integration is recognized as an enabling technology for future ICs and low-cost micro/nano/electro-opto/bio heterogeneous systems. Detailed benefits are explored in many publications and summarized below.

3D Integration Approaches and Worldwide Research Activities

Various 3D technologies are currently pursued, as shown in Figure 2. They can be divided into three categories based on their similarity to other technologies: (1) 3D packaging technology (Figure 2(a-c)); (2) transistor buildup 3D technology (Figure 2(d-f)); and (3) monolithic, wafer-level, back-end-of-the-line (BEOL)-compatible 3D technology (Figure 2(g-k)). Each 3D technology is briefly described below, with some academic or industrial organization names, as examples, showing the worldwide research and development activities:

(a) Packaging-based 3D integration enabled by wire bonding and flip-chip bonding as shown in Figure 2(a). These include system-in-package (SiP), which is formed by stacking thinned chips with wire bonding to connect them, and package-on-package (PoP), which is formed by stacking packages such as SiPs with flip-chip bonding. These SiPs or PoPs are already commercially available products (e.g., from Amkor in the U.S. and STATS ChipPAC in Singapore). Today's new cell phones have at least one SiP or PoP.

(b) Die-to-die 3D integration enabled by thinned die-to-die bonding and through-silicon-via (TSV) interconnections as shown in Figure 2(b). The TSVs are typically formed by laser drill (e.g., prototype eight-die memory stack by Samsung in Korea) or deep reactive-ion-etching (deep-RIE, such as a Bosch process) (e.g., University of Arkansas in the U.S. and ASET in Japan), followed by copper fill.

(c) Die-to-wafer 3D integration, as shown in Figure 2(c), enabled by die-to-wafer bonding, with interchip electrical interconnections formed by post-bond via formation (e.g., Ziptronix in the U.S.) or solder (or eutectic) bonding during the die bonding process (e.g., Fraunhofer IZM in Germany). This approach uses techniques from both packaging and wafer fab, such as die pick-and-place and TSV formation, respectively.

(d) Transistors formed inside the on-chip interconnect layer on a piece of recrystallized silicon film as shown in >>

>> Figure 2(d). A small piece of amorphous silicon film is deposited with a catalyst followed by either laser heating or rapid thermal anneal to recrystallize the silicon. The transistors are then formed by BEOL compatible processing (e.g., Stanford University in the U.S.).

(e) Transistors formed on poly-silicon films layer by layer with tungsten interlayer vias as shown Figure 2(e). After the first layer of transistors is completed, an amorphous silicon film is deposited and converted to poly-silicon (e.g., MATRIX SEMI in the U.S.). The tungsten via can tolerate the relatively high temperatures (~600 C) needed for poly-silicon conversion and transistor formation.

(f) Transistors formed on single-crystal silicon films layer by layer as shown Figure 2(f). The silicon layer can be bonded onto the oxide surface of a previously fabricated transistor layer by transferring the crystal silicon film from a silicon-on-insulator (SOI) wafer. The interstrata via is filled with poly-silicon and/or tungsten, enabling device fabrication at relatively high temperature (e.g., Samsung in Korea).

(g) Wafer-level BEOL-compatible 3D hyper-integration enabled by wafer alignment, bonding, thinning and interwafer interconnections as shown in Figure 2(g-k). All approaches shown use TSVs to form the interstrata interconnections. They differ as to when the via is formed, before/during bonding (via-first) or after bonding (via-last). In addition, a variety of bond layer types can be chosen. Four major bonding and interstrata interconnection approaches are highlighted in Figure 2(h-k):

- via-last, oxide-to-oxide bonding (Figure 2(h)),
- via-last, adhesive (polymer) bonding (Figure 2(i)),
- via-first, copper-to-copper bonding (Figure 2(j)), and
- via-first, metal/adhesive redistribution layer bonding (Figure 2(k)).

Academic and industrial organizations are actively developing a variety of wafer-level 3D technologies, such as Lincoln Lab, MIT, Rensselaer Polytechnic Institute (RPI), the University at Albany, Freescale, IBM, Intel, SEMATECH and Tezzaron in the U.S.; CEA-LETI, Fraunhofer and IMEC in Europe; and Tohoku University in Asia. Many organizations are currently evaluating competing wafer-level 3D technologies.

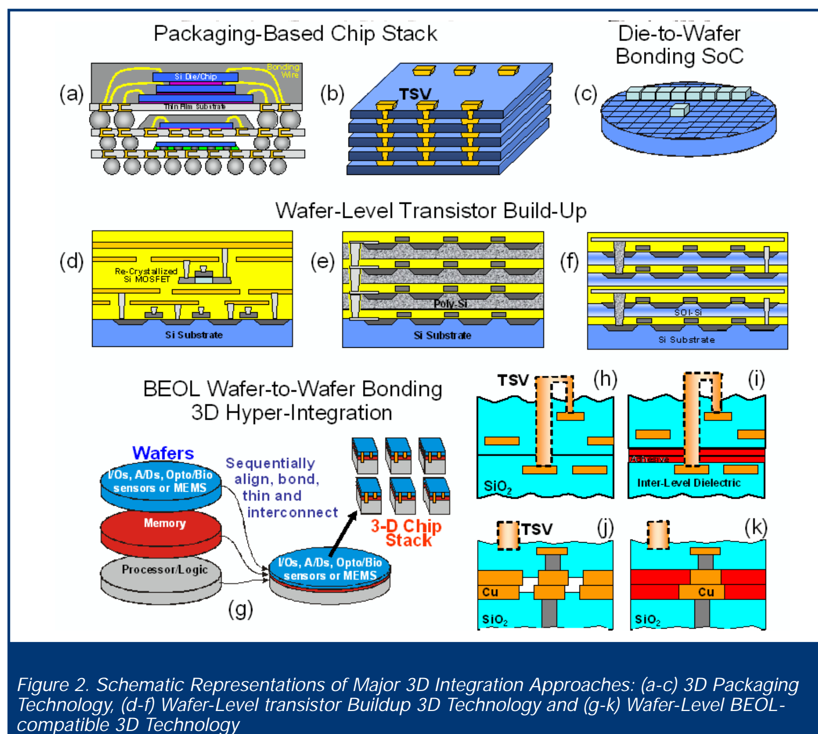

Figure 2. Schematic Representations of Major 3D Integration Approaches: (a-c) 3D Packaging Technology, (d-f) Wafer-Level transistor Buildup 3D Technology and (g-k) Wafer-Level BEOL-compatible 3D Technology

There are also other approaches that are not shown in Figure 2, such as forming the TSVs during the front-end-of-the-line processing (Tezzaron), stacking chips with metallization on the stack side (Irvine Sensors in the U.S.), stacking chips on silicon carrier with TSVs (IBM) or combining various approaches.

Technology Comparison and Applications

We briefly discuss the advantages and limitations of various 3D technologies and their potential applications; a full comparison among 3D technologies is beyond the scope of this article. In general, all 3D technologies would offer *high density* component integration with

- small form factor (small size and light weight);
- reduced packaging; and
- reduced power (fewer I/Os to be driven).

For 3D packaging technologies (Figure 2(a-c)), using known good die (KGD) can provide a yield advantage. Time-to-market for a new product is short because flexibility in the assembly process requires less design effort for a new system. However, the cost for high-volume production can be high because of the testing required for KGDs and the low throughput of pick-and-place assembly. The SiP and PoP approaches (Figure 2(a)) are used in portable devices (e.g., cell phones). The die-stack approach with TSVs (Figure 2(b)) has been demonstrated for memory stacks. The die-wafer approach (Figure 2(c)) has the potential for building 3D SoCs.

Transistor buildup 3D technology (Figure 2(d-f)) can achieve the highest density of Si transistors with wafer-level fabrication using advanced photolithography. Wafer-level processing can also reduce costs for high-volume production. However, the processing constraints (particularly the thermal budget) affect the properties of the transistors and limit the material choices mostly to silicon and tungsten. The Si recrystallization approach (Figure 2(d)) could be used for fabrication of repeaters within interconnect to alleviate interconnect delay. The poly-Si layer approach (Figure 2(e)) is used for low performance memory. The bonded crystal Si approach (Figure 2(f)) can be used for an NAND flash memory

stack. Companies such as Samsung that manufacture cell phones and handhelds see great potential for a high-density memory stack.

For wafer-level BEOL-compatible 3D technology (Figure 2(g-k)), the electrical, RF, optical, thermal and mechanical behavior can be considered for each component separately. For example, the starting yield can be improved by fabricating logic and memory on separate wafers with optimized materials and process technologies. The separate wafers are then stacked using a monolithic wafer-level BEOL-compatible process for all components, potentially improving the cost and overall system yield at high-volume production. Typically the bottom wafer retains its full thickness and serves as a mechanical support for the stack. Each subsequent wafer is then thinned to micron scale after stacking (bonding), thus the overall stack thickness is close to that of a single wafer and can be processed and packaged with current wafer technologies. Massive (millions), short (micron-scale) interwafer interconnects (vias) provide extremely high data bandwidth and dramatically decrease interconnect delay and power consumption.

BEOL-compatible 3D hyper-integration is perhaps the most attractive 3D technology due to its flexibility for heterogeneous integration of different materials, processing technologies and functional components with additional benefits in cost and performance. Many research groups are exploring its potential applications, such as improving interconnect delay (George Institute of Technology (GaTech), MIT, RPI and Stanford in the U.S., and IMEC and Infineon in Europe), memory stacks (Cornell, RPI and Tezzaron in the U.S.), memory-processor or logic-logic stacks (IBM, Intel, Freescale, Tezzaron and RPI in the U.S.), signal processing circuits (GaTech and North Carolina State University in the U.S.), field programmable gate arrays (FPGAs) (MIT and the University of Minnesota in the U.S.), imagers (Lincoln Lab and RTI International in the U.S.), mixed-signal and RF applications (RPI) and 3D power delivery (RPI). Design and simulation tools have been demonstrated for this 3D technology, such as for ECAD tools (Lincoln Lab, MIT, R3 Logic in the U.S.), switching energy, and thermal and mechanical simulations (Intel, MIT, and RPI in the U.S.).

3D Integration Perspectives

Various 3D approaches may be combined to offer more flexible integration with even higher functionality. For example, stacking discrete die (or discrete devices, such as solid-state lasers or GaN transistors) onto a wafer stack provides a pathway for the integration of compound semiconductor devices or analog circuits with digital circuits.

Looking forward, the first killer 3D applications would be extremely high-density heterogeneous memory stacks (e.g., NAND flash, SRAM, DRAM, FRAM and phase change memory) and extremely high-resolution/low-cost imagers. Advanced portable devices will also continue to drive the mix and match of various 3D approaches.

Once 3D integration technology is mature and the manufacturing infrastructure (such as ECAD tools, fabrication equipment and standards) is in place, it is likely that more ICs will be designed for general purposes, because massive production of 3D ICs would lower the manufacturing cost. For instance, a *general-purpose* 3D multi-core processor (with extremely high-density memory, FPGA and software in the nonvolatile memory in the same stack) could be reprogrammed by FPGA or software for multiple purposes, or varying purposes, over a processor's lifetime.

As shown in Figure 1, ongoing research and development in 3D integration could lead to a *new paradigm of future technologies for hyper-integration of infotech-nanotech-biotech systems, enabling extremely high functionality, high performance and small size and weight with very low cost*. Different components optimized for energy/power can be integrated, such as processors, memories, wireless communications, special functions of nano-devices and MEMS, and various micro/nano-scale chemical, bio, thermal, mechanical, electrical and optical sensors. In the future, it will not be just a dream that a tiny device can fly, move, see, smell, hear, taste (analyze), feel and "think"; it will be able to interact with other devices and with human beings and their surroundings; it will also perform certain functions, such as for security (e.g., detection of dangerous materials, devices or terrorists) and healthcare (e.g., medical devices and drug discovery). Our daily lifestyle and even our culture may be dramatically changed with a proliferation of this 3D hyper-integration technology.

Acknowledgments

We would like to thank MARCO, DARPA, NYSTAR and SEMATECH for their support. ■

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