SiO2 Free HfO2 Gate Dielectrics by Physical Vapor Deposition


Abstract—HfO2 layers, 25-Å-thick, were grown by cyclic Hf sputter deposition and room temperature oxidation steps on chemically oxidized Si(001). Subsequent in situ annealing and TiN deposition yields a high-κ gate stack for which the original 8-Å-thick SiO2 layer is eliminated, as confirmed by transmission electron microscopy. Transistors fabricated with this gate stack achieve an equivalent oxide thickness in inversion $T_{\text{inv}} = 9.7$ Å, with a gate leakage $J_g = 0.8$ A/cm$^2$. Devices fabricated without in situ annealing of the HfO2 layer yield a $T_{\text{inv}}$ which increases from 10.8 to 11.2 Å as the oxidation time during each HfO2 growth cycle increases from 10 to 120 s, also causing a decrease in $J_g$ from 0.95 to 0.60 A/cm$^2$, and an increase in the transistor threshold voltage from 272 to 294 mV. The annealing step reduces $T_{\text{inv}}$ by 1.5 Å (10%) but also increases the gate leakage by 0.1 A/cm$^2$ (30%), and causes a 61 mV reduction in $V_t$. These effects are primarily attributed to the oxygen-deficiency of the as-deposited HfO2, which facilitates both the reduction of an interfacial SiO2 layer as well as a partial phase transition to a high-κ cubic or tetragonal HfO2 phase.

Index Terms—HfO2, High k dielectrics, Interface scavenging, SiO2 Interlayer, MOSFET, PVD

I. INTRODUCTION

The leakage current across a SiO2 gate dielectric increases by approximately one order of magnitude for every 2 Å of thickness reduction [1]. In order to enable further device scaling, HfO2 has replaced SiO2 as the gate dielectric in some advanced CMOS transistors, due to its higher dielectric constant ($\kappa_{\text{HfO2}} = 18-20$ vs $\kappa_{\text{SiO2}} = 3.9$) and thermodynamic compatibility with silicon. However, various researchers report the spontaneous formation of an interfacial SiO2 or HfSiO2 layer that develops between the Si substrate and the deposited HfO2 film [2][3][4][5][6]. The most common approach to suppress the spontaneous growth of an interfacial oxide is to deliberately grow an interfacial SiO2 layer prior to HfO2 deposition. This yields better control of the properties of the interfacial layer and provides a more stable surface for nucleation of the HfO2 [7][8]. However, it reduces the overall dielectric constant of the combined stack as, for example, replacing 25% (5 Å) of a 20-Å-thick HfO2 film with SiO2 reduces the effective $\kappa$ of the gate dielectric by ~50%.

Atomic layer deposition (ALD) is the predominant technique used to deposit HfO2 because it provides conformal coverage of three-dimensional structures [9][10] and yields consistent performance in manufacturing environments [11]. Alternatively, physical vapor deposition (PVD) of HfO2 layers has also been reported, including reactive sputtering of Hf in an oxygen ambient [12][13] and sputtering of metallic Hf followed by a high temperature oxidation step [7][14]. Both approaches result in the formation of an interfacial SiO2 layer with a thickness of at least 1.5 nm. Ref. [7] also shows that r.f. magnetron sputter deposition of an un-oxidized Hf metal layer by itself does not result in the formation of an interfacial layer on a native oxide/Si substrate and that the native oxide may be removed during such a deposition. This possible removal of the interfacial SiO2 motivates the present study.

In this paper, we describe a process for depositing HfO2 by PVD which results in thinning of the SiO2 interfacial layer and, combined with post deposition annealing, eliminates a SiO2 layer which is intentionally grown prior to HfO2 deposition. This process enables the production of transistors with a low gate leakage current density $J_g$ of 0.6 A/cm$^2$ at an equivalent oxide thickness in inversion $T_{\text{inv}} < 11.5$ Å. By adjusting the oxidation conditions of the HfO2 layer, both during deposition and in the subsequent anneal, further $T_{\text{inv}}$ scaling down to 9.5 Å is demonstrated with a less than two-fold increase in $J_g$. For this work, 10 μm$^2$ n-channel metal-oxide-semiconductor field effect transistors (NMOSFETs) were fabricated with a HfO2 gate dielectric that was grown using cyclic Hf deposition and room temperature oxidation steps with various oxidation conditions. In order to demonstrate the minimization or absence of the interfacial SiO2 layer, we present TEM micrographs of the gate region of fully processed transistors at various oxidation conditions, as well as the $T_{\text{inv}}, J_g$ and $V_t$ data extracted from the transistors.

II. EXPERIMENTAL PROCEDURE

All samples were prepared in a 300 mm semiconductor development facility. The gate stack consists of a room
temperature chemically grown (HCl) 0.7 nm silicon dioxide layer on a p-type Si(001) substrate. This is followed by deposition of a 2.5-nm-thick HfO₂ gate dielectric and a gate metal consisting of a 5.5-nm-thick TiN and a 100-nm-thick polysilicon layer. The HfO₂ films were grown using 14 deposition-oxidation cycles where each cycle consists of room-temperature sputter deposition of a 1-Å-thick metallic Hf layer in 0.4 mTorr Ar, followed by in situ room-temperature oxidation in the same chamber using a continuous flux of pure O₂ at 50 standard cubic centimeters per minute (scm), which results in a pressure of 0.4 mTorr, for oxidation times \( t_{0.4} \) ranging from 10-120 s. The base pressure of the deposition chamber was less than 1×10⁻⁹ Torr. The number of deposition-oxidation cycles (14) was selected to obtain the desired HfO₂ thickness of 25 Å as measured by ellipsometry on an unannealed uncapped blanket HfO₂ layer, and was held constant for all samples in this study. \( t_{0.4} \) was varied for different sample sets to vary the degree of oxidation. The TiN gate metal was deposited immediately following the HfO₂ in an adjoining process chamber without breaking vacuum, using reactive sputtering at room temperature. Some samples were vacuum annealed at 750 °C for 5 minutes in a 3rd adjoining process chamber with a base pressure 3×10⁻⁹ Torr. Annealing was done after the HfO₂ deposition but prior to the TiN deposition, without breaking vacuum between any of these three processing steps.

NMOSFETs measuring 10 μm² were fabricated using a standardized gate first process flow. The active area for devices was separated by shallow trench isolation, the wells implanted with 1×10¹⁷ cm⁻³ boron, followed by annealing at 1000 °C for 5 s. The gate stack was then formed as described above. After breaking vacuum from the gate stack processing, 100 nm of amorphous silicon was deposited on the TiN surface, followed by reactive ion etching to pattern the gate. Arsenic was implanted to dope the source and drain regions, followed by a 1077 °C spike anneal to activate the dopants. NiPt silicide contacts were made to the source, drain and gate, using a self-aligned silicide (salicide) process. Copper metallization was used to create the wiring between the device terminals and the on-chip electrical probe pads. A final 450 °C, 30 minute forming gas (10% H₂) anneal was performed prior to electrical testing.

### III. RESULTS

Figure 1 shows cross-sectional high resolution TEM micrographs from three Si- HfO₂-TiN gate stacks of completed NMOS transistors. Cross-sectional samples were prepared for TEM by a typical “in situ lift-out” method using a 30 keV Ga⁺ focused ion beam (FIB) on a 300 nm full wafer Scanning Electron Microscopy / Focused Ion Beam (SEM/FIB) dual beam system. Ion beam damage of the device gate stack was prevented by encapsulating the wafer with a 100 nm amorphous Si film prior to cross-section preparation. A low energy (5 keV) Ga⁺ ion beam was used for final polishing to reduce the amorphization damages on the sample surfaces. High-resolution TEM (HRTEM) analysis was performed on a scanning transmission electron microscope (S-TEM) operated at 200 keV. The HfO₂ layer appears in the micrographs as relatively dark contrast, due to the high atomic mass of Hf, and is in between the single-crystal Si(001) substrate at the bottom of the micrograph and the polycrystalline TiN metal gate at the top. The dotted horizontal lines indicate the positions of transitions from crystalline-to-amorphous and amorphous-to-crystalline microstructures, as determined from an analysis of the atomic positions in larger micrographs than what is shown in Fig. 1. The distance between these two interfaces in Fig. 1(a) is 26.0±0.8 Å, which corresponds to the total dielectric thickness. However, the bottom 8.4±1.2 Å of the dielectric appear considerably brighter, indicating that this fraction of the layer has a lower average atomic mass, which is attributed to the bottom of the dielectric layer consisting of SiO₂ (or SiO₂+HfO₂) rather than HfO₂. That is, the specimen shown in Fig. 1(a) exhibits a 8.4±1.2 Å thick interfacial SiO₂ (or SiO₂+HfO₂) layer between the Si(001) substrate and the deposited HfO₂, consistent with the thickness of the chemically grown oxide prior to the HfO₂ deposition, which was measured by ellipsometry to be 8±1 Å.

The gate stack shown in Fig. 1(b) is processed identically to that shown in Fig. 1(a), except that the oxidation time is reduced by a factor of 12, corresponding to \( t_{0.4} = 10 \) s of oxidation per cycle. The total oxide thickness indicated in the figure by the two lines is 25.4±3.1 Å. This is, within experimental uncertainty, identical to the sample shown in Fig. 1(a). However, the thickness of the bright portion of the oxide is reduced to 4.2±0.3 Å, indicating that the original chemically grown SiO₂ layer has been reduced during the PVD HfO₂ deposition, presumably by oxygen diffusion from the SiO₂ layer to the HfO₂ to recombine with oxygen vacancies created due to the oxygen deficiency during deposition. Fig. 1(c) shows a micrograph from a HfO₂ layer obtained using the same deposition process conditions (with \( t_{0.4} = 120 \) s) as Fig. 1(a), but which was vacuum annealed at 750 °C for 5 min, prior to the TiN deposition. The total dielectric thickness for this specimen is 23.8±0.7 Å. No bright amorphous interfacial layer can be detected, indicating the absence of SiO₂ or a thickness of a possible SiO₂ layer below the detection limit of 2 Å.

In order to further investigate the presence or absence of SiO₂ interfacial layers, local electron energy loss spectra (EELS) were acquired for the three samples shown in Fig. 1. Line scans across the interfaces from the Si substrate to the TiN layer were obtained using a 5 Å step size. O and Hf onsets are then defined as the positions along the measured line where the O and Hf EELS intensities reach half of their maximum measured intensity in the HfO₂ layer, and the relative positions of these onsets is then used as a relative measure of the thickness of an interfacial SiO₂ layer. This analysis shows that the oxygen onset for the sample in Fig. 1(a) occurs 12±5 Å below the Hf onset, suggesting a possible SiO₂ layer with a thickness of 12±5 Å, in reasonable agreement with the 8.4±1.2 Å determined from the micrograph and 8±1 Å for the original chemically grown oxide. The spacing of the EELS onsets decreases to 8±5 Å and 6±5 Å for Figs. 1(b) and (c), respectively. That is, the thickness of the SiO₂ interfacial layer decreases from Fig. 1(a)
to (b) to (c), which is fully consistent with the direct interpretation of the micrographs. We note here that the uncertainty of ±5 Å associated with the finite step size as well as the electron beam size and the broadening due to elastic scattering in the specimen do not allow to quantitatively measure the SiO2 thickness. In addition, the used method using the relative positions of the O and Hf onsets results in an additional systematic error of ~10 Å, such that the EELS method can only be used to compare samples rather than to obtain an absolute value for the SiO2 thickness.

Figure 2 shows the electrical performance of transistors fabricated using the PVD HfO2 deposition process for \( t_{O2} \) ranging from 10 to 120 s. The plot in Fig. 2(a) indicates the measured gate leakage current density \( J_g \) for the fabricated \( A = 10 \mu m^2 \) devices vs gate capacitance \( C \) measured at 0.8 V above the threshold voltage \( V_T \) and shown as inversion thickness \( T_{inv} = \kappa_{SiO2}e_2A/C \), where \( \kappa_{SiO2} = 3.9 \) is the dielectric constant of SiO2 and \( e_2 \) is the vacuum permittivity. The inset shows a typical high frequency (1 MHz) capacitance-gate bias \((C-V)\) curve which is used to determine \( C \) and is obtained from a device with a gate stack grown with \( t_{O2} = 30 \) s. The plotted error bars in Fig. 2(a) correspond to the standard deviation in \( J_g \) and \( T_{inv} \), obtained from characterizing transistors from 8-10 different chips on a single wafer for each processing condition. As \( t_{O2} \) is increased from 10 to 120 s, \( C \) decreases from 3.22 to 3.07 pF, corresponding to an increase in \( T_{inv} \) from 10.8 to 11.3 Å. Simultaneously, \( J_g \) decreases by a factor of 1.6, from 0.95 to 0.60 A/cm2. The plot in Fig. 2(a) also shows the data from devices fabricated using \( t_{O2} = 120 \) s and a 750 °C vacuum annealing step between HfO2 and TiN deposition, corresponding to the sample shown in Fig. 1(c) which exhibits no interfacial SiO2. These devices exhibit a considerably higher capacitance, such that \( T_{inv} = 9.6 \) Å, almost 2 Å less than the unannealed samples with the identical oxidation condition, while \( J_g = 0.70 \) A/cm2 is nearly unaffected by the annealing.

Fig. 2(b) is a plot of the transistor threshold voltage \( V_T \) vs the oxidation exposure time \( t_{O2} \). The measured voltage increases from \( V_T = 272 \) mV for \( t_{O2} = 10 \) s to \( V_T = 294 \) mV for \( t_{O2} = 120 \) s, following a logarithmic trend \( V_T \propto \ln(t_{O2}) \), as indicated by the straight line in Fig. 2(b). This trend with \( t_{O2} \) suggests that \( V_T \) is related to the degree of oxidation of the metallic Hf layer, since the low temperature oxidation of many metals is known to follow a logarithmic growth law [15]. The figure also includes the threshold voltage for devices with \( t_{O2} = 120 \) s that were annealed at 750 °C between HfO2 and TiN deposition. The measured \( V_T = 233 \) mV, which is 61 mV below the value for samples fabricated with the same oxidation exposure time but without annealing.

IV. DISCUSSION

The data presented in Fig. 1 demonstrates that the PVD HfO2 deposition conditions affect the final thickness of the interfacial SiO2 layer, with smaller \( t_{O2} \) yielding thinner SiO2 layers. Additionally, post deposition vacuum annealing causes the interfacial SiO2 to be completely eliminated. The transistor electrical performance data in Fig. 2 show that \( J_g \) and \( T_{inv} \) are also affected by the HfO2 deposition conditions. In particular \( J_g \) decreases and \( T_{inv} \) increases with increasing \( t_{O2} \), while vacuum annealing significantly reduces \( T_{inv} \) with an increase in \( J_g \) that is much smaller than what would be expected from an exponential dependency of \( J_g \) on \( T_{inv} \). The observed trends with \( t_{O2} \) in Figs. 1 and 2 can be attributed to an increasing oxidation time during HfO2 formation leading to a smaller fraction of the SiO2 being reduced, yielding a thicker SiO2 interfacial layer and therefore a larger \( T_{inv} \) as well as a smaller \( J_g \). The latter effect is amplified by an increased electron tunneling barrier since SiO2 has a higher bandgap than HfO2. With a similar argument, we attribute the complete removal of the interfacial SiO2 layer during annealing to the reduction of SiO2, which in turn results in a reduced \( T_{inv} \). However, the reduction in \( T_{inv} \) is much larger than the changes observed for different \( t_{O2} \), and more importantly, the data point for the annealed samples in Fig. 2 does not fall on the line of the \( J_g \) vs \( T_{inv} \) trend from the transistors without HfO2 anneal. Therefore, we attribute the decrease in \( T_{inv} \) during annealing to an increase in the dielectric constant of the HfO2 layer. A similar increase in \( \kappa \) has previously been reported during annealing of a Ti-covered HfO2 layer [16], and has been attributed to oxygen diffusing to the Ti, which facilitates a transition from a readily formed monoclinic phase with \( \kappa = 18 \) to a cubic phase with \( \kappa = 40 \). Similarly, we postulate that oxygen deficient HfO2 in our samples facilitates the phase transition to a cubic or tetragonal high-\( \kappa \) phase during annealing [17]. This explanation is also consistent with the measured \( J_g \) remaining approximately constant during annealing, which, in turn, suggests that the thickness of the insulating oxide (SiO2-HfO2) remains approximately constant. In fact, the measured thicknesses of the devices in Figs. 1(a) and (c) are 26.0±0.8 and 23.8±0.7 Å before and after annealing, respectively, which corresponds to only a 2.2±0.5 Å (8±5%) decrease. In contrast, \( T_{inv} \) decreases by 15% from 11.3 to 9.6 Å, corresponding to an increase of the effective \( \kappa \) from 11.7 to 13.9, determined assuming a constant oxide thickness of 23.8 Å and channel inversion layer thickness of 10.2 Å. These \( \kappa \) values are considerably lower than the reported bulk values of 18 for monoclinic HfO2, 40-50 for cubic HfO2 and 70 for tetragonal HfO2 [16][18][19]. This is expected for the unannealed film, considering the interface layer with a significantly lower \( \kappa \); but suggests that a relatively small portion of the annealed film is converted to the cubic phase, and that even the annealed film contains residual structural defects including oxygen vacancies within the HfO2 layer or at the interfaces, and/or interface roughness reduces the effective \( \kappa \).

A similar increase in \( \kappa \) during annealing has been previously reported for HfO2 deposited by room temperature reactive sputtering and has been attributed to the presence of short range cubic ordering which is already present in the as-
deposited amorphous HfO₂ and facilitates development of the higher-κ cubic phase during extended vacuum annealing [20]. Alternatively, the increase in κ could be attributed to Si atoms that are liberated by the reduction of the SiO₂ interfacial layer, diffuse into the HfO₂, and help to stabilize the tetragonal phase. This tetragonal phase stabilization has been reported for doping of HfO₂ with several elements, including Zr [21] and Y [17], but most notably (for our work) Si, which was described by Tomida et al. [22] for direct deposition of low (~10%) Si hafnium silicate films as high κ layers. If all Si from the initial SiO₂ layer would diffuse into the HfO₂, we expect a Si:Hf ratio of 1:3, as estimated based on the relative thicknesses of the initial SiO₂ and the as-deposited HfO₂ layers. However, our EELS analysis shows no evidence for Si (< 10 at.%) in the HfO₂, indicating that diffusion into the HfO₂ is not the primary path for Si atoms, consistent with other reports on the SiO₂ interfacial layer dissociation [23][24], suggesting that the liberated silicon atoms mostly re-incorporate into the substrate crystal, with only a minimal amount of Si diffusing into the HfO₂ layer. Nevertheless, since only a small Si concentration is required to facilitate the phase transformation, Si diffusion may also play a role in the increase of κ during the annealing of our HfO₂ layers.

The $V_i$ shift with oxidation condition, shown in Fig. 2(b), supports the conclusion that the as-deposited film is incompletely oxidized. In particular, the increase in $V_i$ suggests a decrease in oxygen vacancies with increasing $t_{ox}$ [25]. This is because the positive charge associated with oxygen vacancies reduces the positive voltage required to invert the charge in the channel to turn a transistor on. Thus, the positive slope of $V_i$ vs $t_{ox}$ in Fig. 2(b) directly indicates that an increase in $t_{ox}$ results in an increase in $x$ for the deposited HfO₂. Correspondingly, $V_i$ of the annealed device is 61 mV lower than that of the un-annealed sample at the same $t_{ox} = 120$ s, which is attributed to the creation of additional oxygen vacancies during the vacuum anneal, causing an increase in the positive charge in the HfO₂ layer.

V. CONCLUSIONS

We have developed a novel process for depositing HfO₂ using cyclic PVD Hf deposition and oxidation. Planar transistors that are fabricated with this process exhibit a low $T_{inv}$ and $J_g$, which can be controlled by both adjusting the oxidation conditions during deposition and performing a post-deposition vacuum anneal of the HfO₂ layer. Decreasing $t_{ox}$ causes a reduction in $T_{inv}$ and $V_i$, but an increase in $J_g$. A 750 °C vacuum anneal following deposition significantly reduces $T_{inv}$ but increases $J_g$ and causes a $V_i$ shift of -61 mV. Additionally, TEM analyses indicate that a reduction in $t_{ox}$ causes a reduction of the SiO₂ layer thickness at the Si-Hf interface, and that annealing completely eliminates the interfacial SiO₂ layer of a fully processed transistor. The changes with $t_{ox}$ are attributed to oxygen deficiencies in the as-deposited HfO₂, which enable the reduction of the pre-existing SiO₂ interfacial layer, while annealing causes an additional partial phase transformation from the lower κ monoclinic phase to the higher κ cubic or tetragonal phases, which is also facilitated by the oxygen-deficiency of the as-deposited HfO₂.

REFERENCES


Figures

**FIG. 1.** Transmission electron micrographs showing the gate regions of transistors with PVD HfO₂ deposited using cyclic Hf-oxidation with an oxidation time $t_{\text{ox}}$ per cycle of (a) 120 s and (b) 10 s. (c) 120 s (same condition as in (a), but processing includes annealing in vacuum at 750 °C for 5 min prior to TiN deposition).

**FIG. 2.** (a) Gate leakage current $J_g$ vs. inversion thickness $T_{\text{inv}}$ as determined from the measured capacitance $C$ of transistors with a HfO₂ gate dielectric grown using an oxidation time per deposition cycle $t_{\text{ox}}$ = 10, 30, 60, and 120 s, and from an annealed sample with $t_{\text{ox}} = 120$ s. The inset is a typical high frequency capacitance-gate bias ($C-V$) plot from a device grown with $t_{\text{ox}} = 30$ s. (b) Threshold voltage $V_t$ vs. $t_{\text{ox}}$. 